

SERVICE MANUAL

AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

Prepared by

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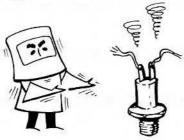
## SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to dangerous electrical shock when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:



1 Do not attempt to adjust unprotected circuit controls or to dress leads with power on.



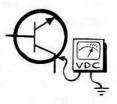
2 Do not touch heavily loaded or overheated components without precaution to avoid burns.



3 Do not assume that all danger of electrical shock is removed when power is off. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.



4 Always avoid placing parts of the body in series between ground and circuit points.



5 Remember that some semiconductor cases and solid-state circuits carry high voltages.



6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, turn power off before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

#### WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS REMOVED OR YOU MAY ALSO BECOME A SHOCK VICTIM.

If power cannot be removed immediately, very carefully loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

### **GOOD PRACTICES**

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

- 1 When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.
- 2 When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.
- 3 When troubleshooting, remember that FETs and other metal-oxidesemiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.
- 4 When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.
- 5 When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

#### WARNING

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

#### Charles State St.

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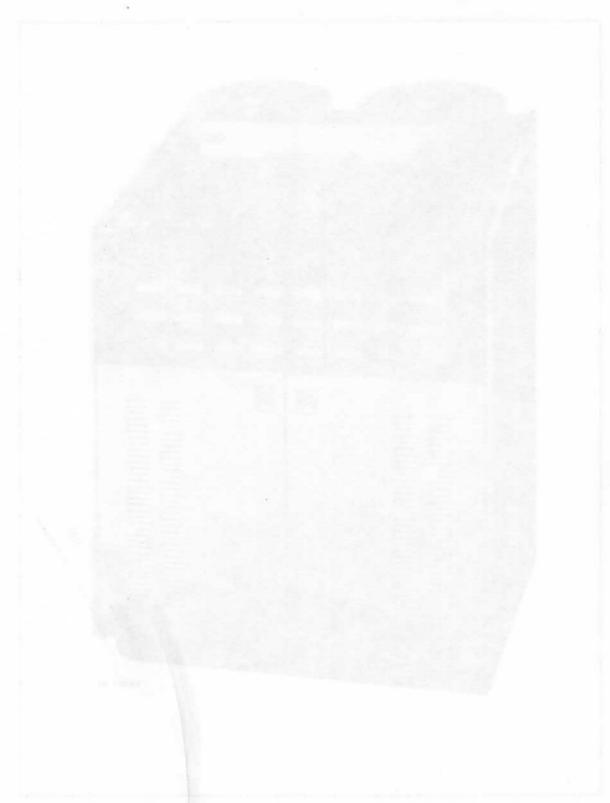
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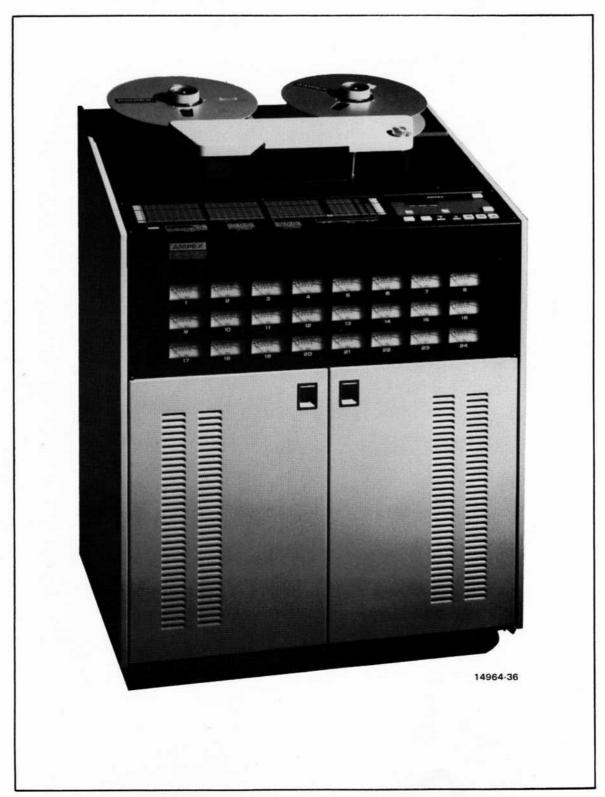
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ATR-116/124 Multichannel Recorder/Reproducer

# SECTION 1 GENERAL INFORMATION

#### 1-1 PURPOSE AND SCOPE OF MANUAL

This manual provides general information, installation procedures, theory of operation, maintenance instructions, and schematics for the ATR-116/124 Multichannel Recorder/Reproducer, Ampex Part No. 4010340.

### 1-2 EQUIPMENT USE

The ATR-116/124 is professional quality, multichannel recorder/reproducer intended for use wherever a high-quality recorder/reproducer is required.

#### 1-3 EQUIPMENT CAPABILITIES

The Ampex ATR-116/124 provides up to 24 channels of audio recording/reproducing capability. The machine operates in any of three speeds: 7.5 in/s, 15 in/s, 30 in/s.

The ATR-116/124 provides, through Sel Sync<sup>(1)</sup> (Selective Synchronization), the capability of recording on one or more channels simultaneously while monitoring one or more non-adjacent, previously-recorded channels. This capability is exercised by using the record head of a previously recorded channel in a playback mode while using one or more other channels in the record mode.

The ATR-116/124 recorder/reproducer, shown in the frontispiece, includes a tape transport assembly, a head assembly, audio electronics assemblies, control assemblies, a power supply assembly, a meter panel assembly, and an input/output panel assembly. Multipin connectors are used extensively between units to facilitate removal and replacement of various components and assemblies. Forcedair circulation is also provided to dissipate heat generated when the recorder is in use. Location of the various components and assemblies is shown in Figures 1-1 through 1-8.

The recorder/reproducer does not incorporate a capstan pinchroller. Tape movement in all modes of operation is under capstan and reel servo control. The capstan servo controls speed and direction while the reel servo maintains dynamically constant tape tension.

The ATR-116/124 incorporates such standard features as an electronic tape timer, search-to-cue, PURC<sup>(1)</sup> (Pick-Up Recording Capability), dynamic braking, audio test circuit, and membrane setup panel. The tape timer displays in hours, minutes,

<sup>(1)</sup> Ampex Trademark

and seconds the distance the tape has moved from a zero reference point. The search-to-cue feature provides automatic access to a preprogrammed point on the tape for editing. The PURC feature eliminates the problem of overlaps and holes in recordings when inserting (dubbing) new material within previously recorded programs. The system does not have mechanical brakes but incorporates dynamic braking to control all braking functions including stopping tape motion when power is removed. The audio test circuit provides I/O channel selection and connectors at the front of the machine for servicing and equalization setup.

#### 1-4 TAPE TRANSPORT

All components of the tape transport (Figure 1-1) are mounted on a rigid, precision-machined, cast-aluminum base. The tape transport consists mainly of subassemblies which are easily removed and installed. Electrical connections are made by harness connectors, thereby eliminating the need for soldering.

Basic components of the tape transport are the capstan, supply and take-up motors, supply and take-up tension arms, tape lifters, and tape-timer tachometer assembly. Tape motion is controlled in all modes of operation (including fast forward and rewind) by the capstan and reel servos. The capstan meters the tape and the tension arms supply arm position (and therefore tape tension) information to the reel servo system. This arrangement results in virtually constant tape tension in all modes of operation.

Tape motion causes the tape-timer tachometer to rotate; a photoelectric device, located below the tape-timer tachometer, provides rotational information to the tape-timer circuitry.

Tape speed is selected by operating a membrane switch located on the tape transport. This switch allows the PURC timing and tape-timer circuitry to be switched according to speed selected.

The transport accommodates tape reels up to 16 in. (40.6 cm) in diameter on either side and in any combination.

During fast forward and rewind modes, two solenoid-actuated tape-lifter arms automatically lift the tape from the heads. For editing and cueing operations, override of the tape-lifter arms is provided by pressing the LIFT DEFEAT pushbutton.

#### 1-5 HEAD ASSEMBLY

The head assembly is a self-contained unit. Three head assemblies (8-track, 16-track, and 24-track) are available for use with the ATR-116/124 in the standard configuration. The 16-track and 24-track head assemblies are used with 2-in. tape. Each head assembly contains three headstack assemblies: the erase head, the record head, and the reproduce head. The head assembly also contains one scrapeflutter idler. The record and reproduce stacks are magnetically shielded with laminated mu-metal. A hinged head-shield assembly is mounted in front of the record and reproduce heads. In addition, a precision tape guide is mounted

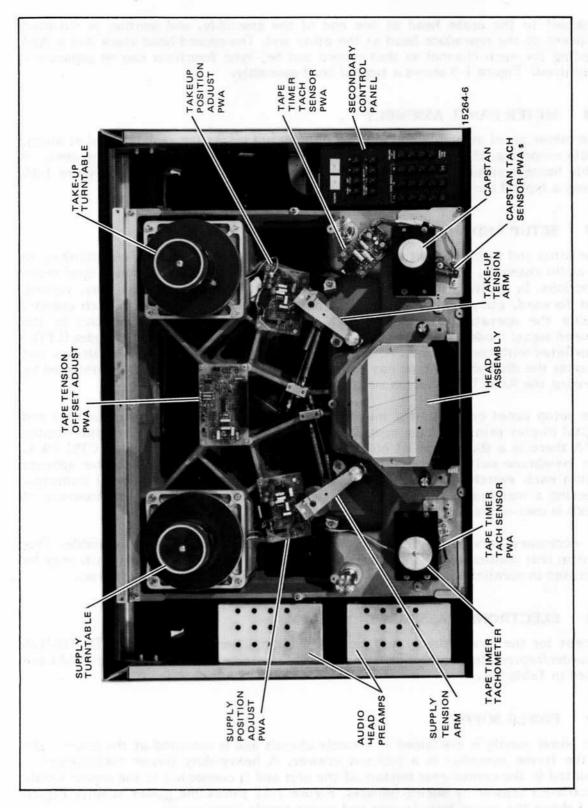


Figure 1-1. Top View of Tape Transport With Overlay Panel and Head Cover Removed

adjacent to the erase head at one end of the assembly, and another is mounted adjacent to the reproduce head at the other end. The record head stack has a dual winding for each channel so that record and Sel-Sync functions can be separately optimized. Figure 1-9 shows a typical head assembly.

#### 1-6 METER PANEL ASSEMBLY

The meter panel assembly contains an illuminated meter for each channel of audio. While recording, the meters are backlighted in red for each channel being used. A cable harness provides interconnection with the electronics assembly. Figure 1-10 shows a typical meter panel assembly.

#### 1-7 SETUP AND MACHINE CONTROL

The setup and machine control panels (Figure 1-11) are capable of controlling up to 24 audio channels, and enable the operator to initiate all transport and signal mode functions. In addition to controlling all transport functions such as play, record, fast forward, etc., membrane (pushbutton) switches associated with each channel enable the operator to program each channel separately for operation in the desired signal mode. Program selection is indicated by light-emitting diodes (LEDs) associated with each channel. A tape-timer display indicates in hours, minutes, and seconds the distance the tape has moved from a zero reference point established by pressing the RESET pushbutton switch.

The setup panel consists of a membrane switch assembly layer over an LED and digital display printed wiring assembly (PWA). Beneath the LED and digital display PWA there is a third layer of electronics consisting of a control panel CPU PWA. The membrane switches are translucent so their associated LED indicator appears within each switch. This gives a visual indication that the function is actuated. Pressing a membrane switch can also generate an audible tone, the loudness of which is user-adjustable.

An accessory remote control unit with a 25-ft (7.6m) cable is available. This control unit duplicates all functions and displays of the local control unit, may be operated in parallel with the local control unit, and is entirely self-powered.

#### 1-8 ELECTRONICS ASSEMBLY

Except for the power supply and motor drive amplifiers (MDAs), the ATR-116/124 recorder/reproducer electronics are primarily contained on PWAs. These PWAs are listed in Table 1-1.

#### 1-9 POWER SUPPLY

The power supply is contained in a single chassis and is mounted at the lower right of the frame assembly in a pull-out drawer. A heavy-duty power transformer is mounted in the center-rear bottom of the unit and is connected to the power supply electronics drawer by wiring harness. Figure 1-12 shows the power supply; Figure 1-13 shows the power transformer and power supply locations.

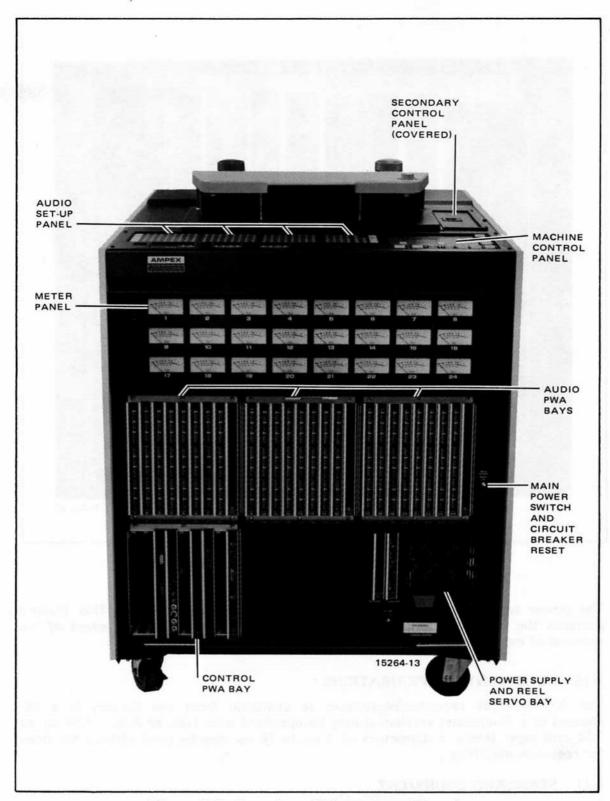


Figure 1-2. Location of Components (Front)

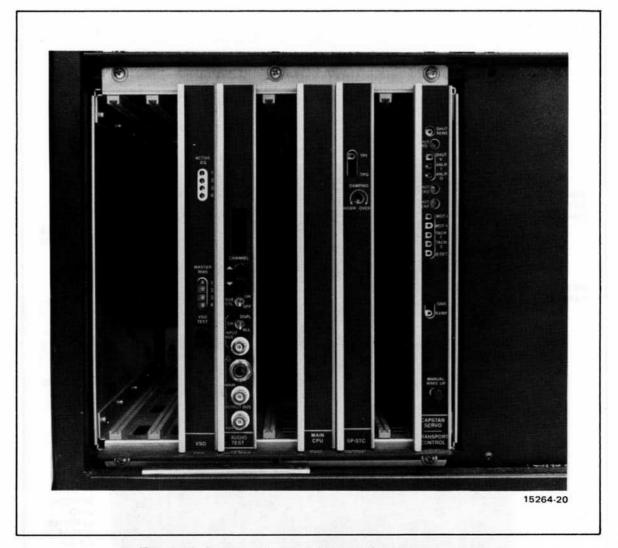


Figure 1-3. Location of Control Bay Components

The power supply contains a battery for the "stay alive" memory. This feature protects the contents stored in the control system memory in the event of the removal of external power for any reason.

#### 1-10 EQUIPMENT CONFIGURATIONS

The ATR-116/124 recorder/reproducer is available from the factory in a 16-channel or a 24-channel version. It may be operated with 1-in. or 2-in. (2.54 cm or 5.08 cm) tape. Reels in diameters of 5 in. to 16 in. may be used without the need for reel-size matching.

#### 1-11 STANDARD EQUIPMENT

Standard equipment supplied with the ATR-116/124 is listed in Table 1-2.

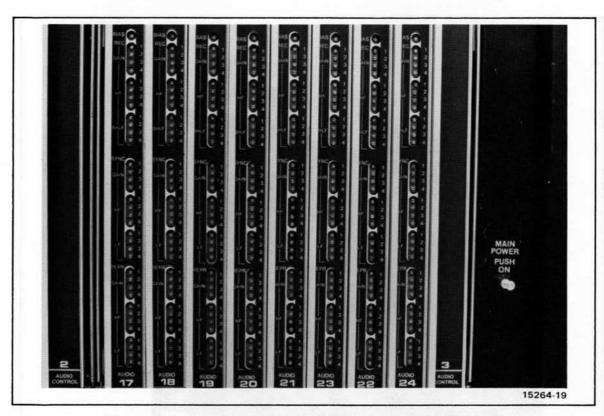


Figure 1-4. Location of Audio Bay Components (Typical)

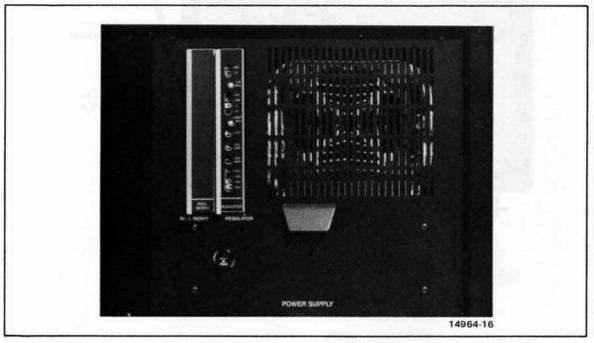


Figure 1-5. Location of Power Supply and Reel Servo Bay Components

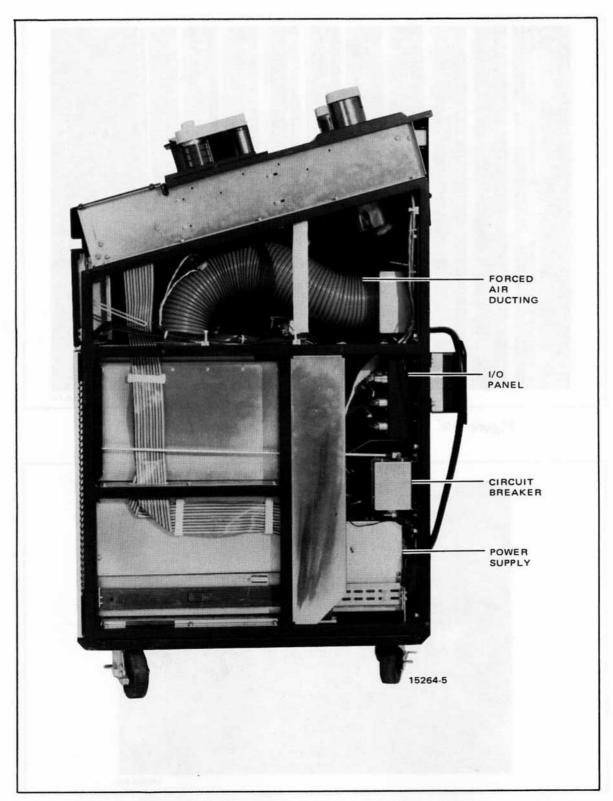


Figure 1-6. Location of Components (Right Side)

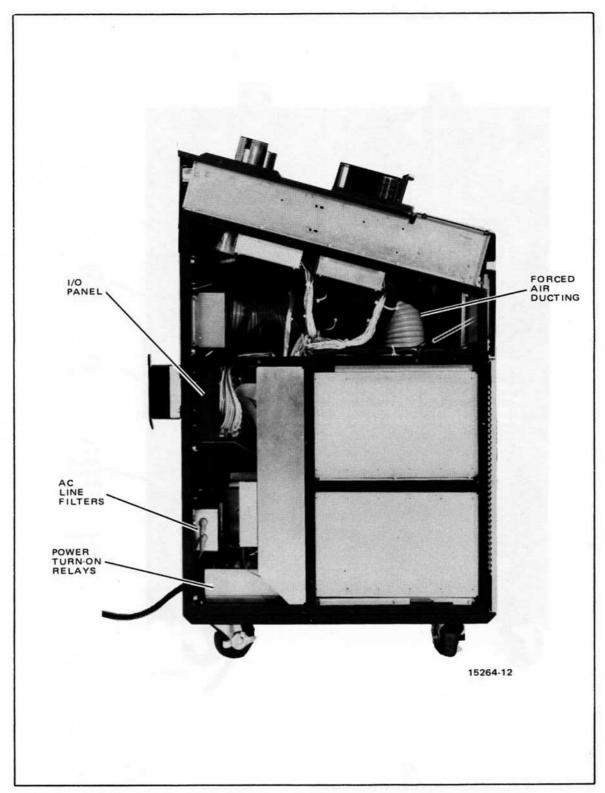


Figure 1-7. Location of Components (Left Side)

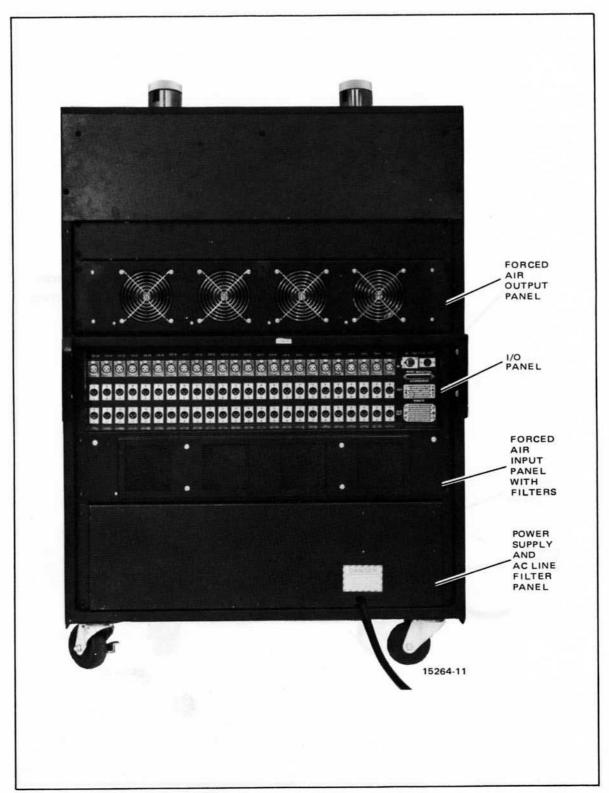


Figure 1-8. Location of Components (Rear)

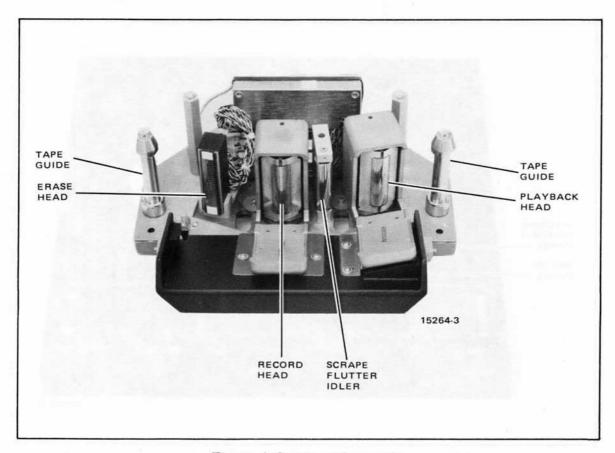


Figure 1-9. Head Assembly

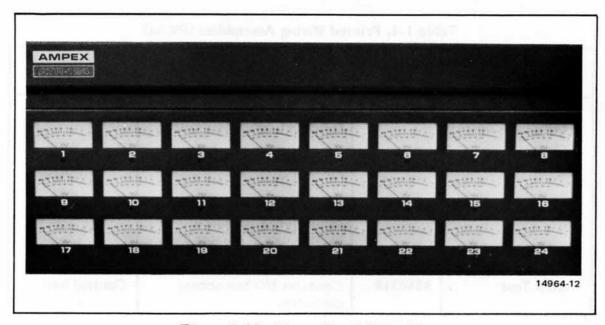


Figure 1-10. Meter Panel Assembly

Ampex 4890425-01

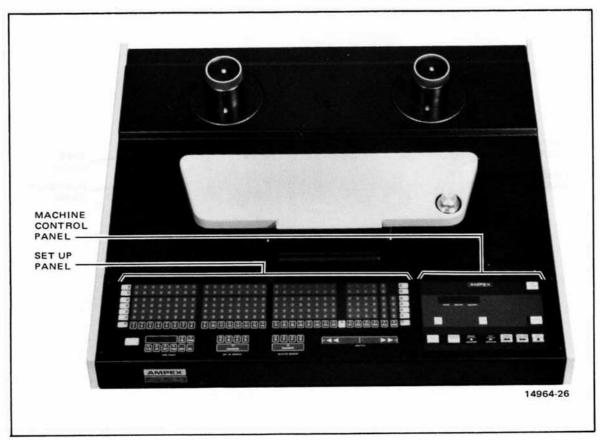


Figure 1-11. Setup and Machine Control Panels

Table 1-1. Printed Wiring Assemblies (PWAs)

PWA	Schematic No.	Function	Location
Capstan Servo/ Transport Control	4840473	Contains capstan servo/ transport control circuitry.	Control bay
Main CPU	4840543	Contains main CPU circuitry.	Control bay
VSO	4840544	Contains variable-speed oscillator (VSO) circuitry, master clock, master bias, and erase.	Control bay
Audio Test	4840518	Contains I/O bus access circuitry.	Control bay

(Continued next page)

Table 1-1. Printed Wiring Assemblies (PWAs) (Continued)

PWA	Schematic No.	Function	Location	
Audio Test/ Auto Bias	4840519	Contains I/O bus access and auto-bias (option) circuitry.	Control bay	
Tape Timer/SP Search-to-Cue	4840504	Contains tape timer, single- point search-to-cue circuitry.	Control bay	
Capstan Tach Preamp	4840481	Contains capstan tach preamp circuitry.	Transport	
Offset Adjustment	4840480	Contains tension arm offset adjustment circuitry.	Transport	
Supply Position Adjustment	4840480	Contains supply tension arm sensor circuitry.	Transport	
Takeup Position Adjustment	4840480	Contains takeup tension arm sensor circuitry.	Transport	
Preamplifier	4840485	Contains repro and sync preamplifier circuitry for four channels.	Next to transport	
Tape Timer Tach	4840480	Contains tape-timer tach.	Transport	
Reel Servo	4840472	Contains reel servo circuitry.	Power supply	
Regulator	4840499	Contains regulator circuitry for power supply.	Power supply	
Panel CPU	4840589	Contains panel CPU circuitry.	Control panel	
Audio Control	4840492	Controls Audio Signal PWA operation for eight channels.	Audio card bay	
Audio Signal	4840551	Processes audio input and output (one for each channel).	Audio card bay	
	of their	Tree to the same of the same o		

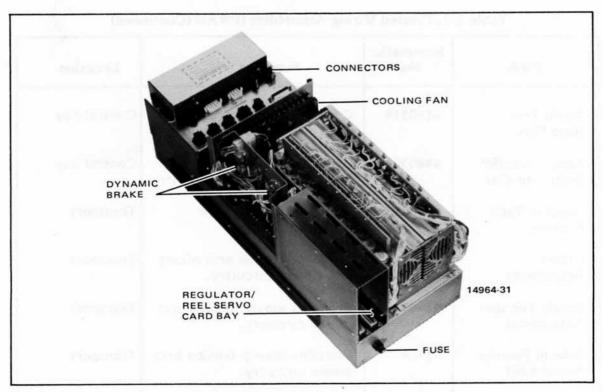


Figure 1-12. Power Supply

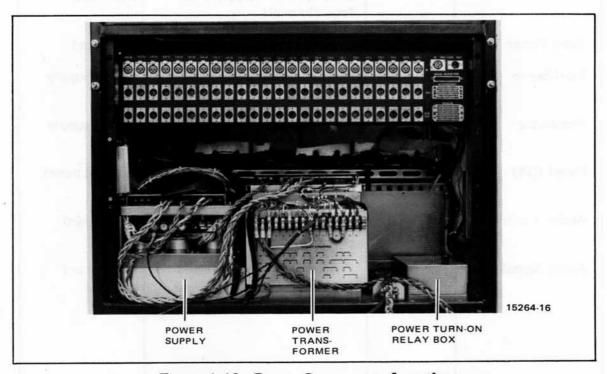


Figure 1-13. Power Components Location

Table 1-2. Standard Equipment (Supplied with Recorder)

Part No.	Description		
4051052-01	PWA-extender board	1	
4050800-01	PWA-extender board	1	
4030467-01	Setup control-panel service fixture	1	
28050-04	Reel, empty 2 in.	1	
4890425-01	Service Manual	1	
145-702	Accessory connector, 75-position	1	
360-478	Alignment tool	1	
360-422	Tool, screwdriver set, hex	1	
167-648	NRT connector, 37-position	1	
167-685	NRT connector pins	40	
167-597	NRT connector hood kit	1	
360-470	NRT connector pin removal tool Amp. 91067-2	1	

#### 1-12 OPTIONAL ACCESSORIES

Table 1-3 provides a list of optional items which are supplementary to standard recorder equipment.

Table 1-3. Optional Accessories

Accessory	Part No.
Audio Test/Auto Bias PWA	4051011
Caster, 2-in. diameter	082-053
Conversion Kit, 8-channel	4010339
Cover, ATR-116/124	4880261
Extender PWA, Swivel	4050975
Flux Loop Assembly, 2-in.	4020484
Flux Loop Equalizing Amplifier	4040424
Head Assembly, 16-channel	4020451
Head Assembly, 24-channel	4020450
Multiple Point Search-To-Cue (MPSTC)	4010306
Power Supply Extender Cable	4051048
Preamp Test PWA	4051078
Remote Control Assembly	4010320
Spares Kit A	1386047
Spares Kit B	1386048
Spares Kit C	1386049
Test Tapes, Audio Signal Alignment	La la la markina
	2001/20

#### 1-13 Audio Test/Auto-Bias PWA

For this accessory (Figure 1-14), the circuitry of the optional auto-bias function and the circuitry of the audio test function are included on the same PWA. The audio test portion is part of the recorder's standard equipment on a separate PWA. The optional auto-bias function automatically sets the biasing of the record head for all 24 channels.

#### 1-14 Eight-Channel Conversion Kit

Provides the added capability of recording and reproducing on 1-in., 8-track tape.

#### 1-15 Two-Inch Flux Loop Assembly

Provides one means of inducing flux into the reproduce head during equalization alignment.

#### 1-16 Flux Loop Equalization Amplifier

Used to provide equalization of the flux loop assembly described above. See paragraph 5-26.

#### 1-17 Multiple Point Search-To-Cue (MPSTC)

Consists of a machine control panel assembly and CPU PWA, Figure 1-15. These components replace the respective standard machine control panel and single point search-to-cue (SPSTC) PWA. The MPSTC is a multi-event editor with a storage capacity for 100 cue points. Refer to Catalog No. 4890426, ATR 116/124 Multiple Recorder/Reproducer, Operation and Maintenance, for a complete description of this option.

### 1-18 Preamp Test PWA

Used to facilitate head preamplifier adjustment. See paragraph 5-49.

### 1-19 Remote Control Assembly

The remote control assembly, Figure 1-16, can be configured to house the setup panel and either the SPSTC or MPSTC machine control panel.

### 1-20 Spares Kit A

Provides backup replacement PWAs for all functions which are needed for basic recorder operation.

### 1-21 Spares Kit B

Provides replacement of active electronic components, i.e. transistors and ICs.

### 1-22 Spares Kit C

Provides for the replacement of moving parts such as motors, movable arms, guides, meters, and solenoids which may not be readily purchased in the area where the recorder is used.

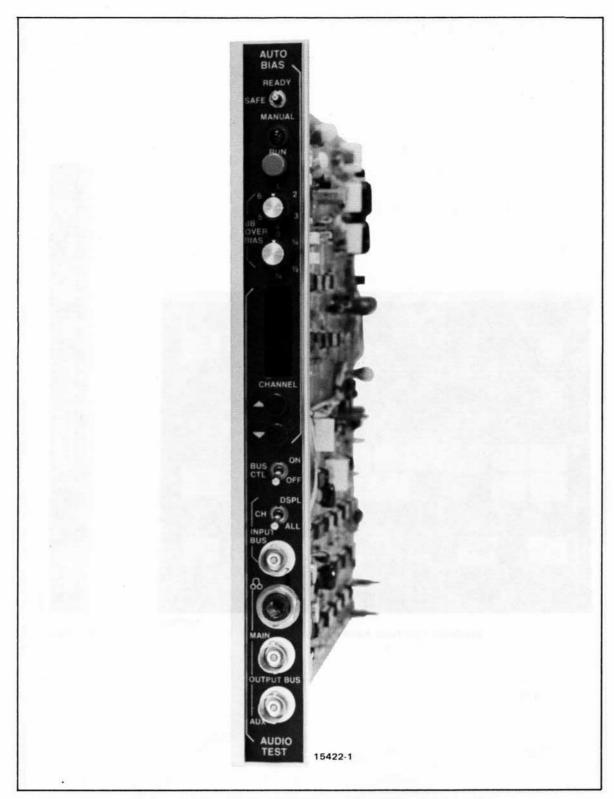


Figure 1-14. Audio Test/Auto-Bias PWA Accessory

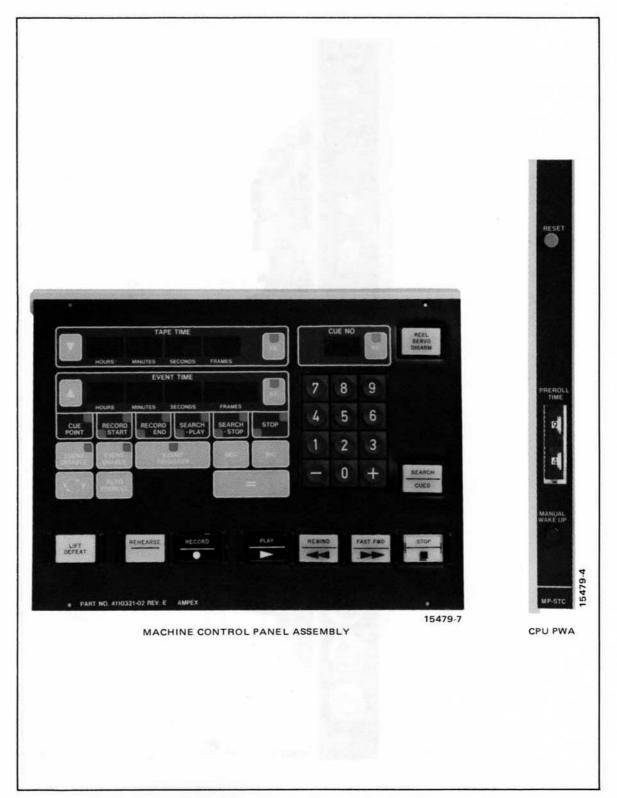


Figure 1-15. Multipoint Search-to-Cue Accessory



Figure 1-16. Remote Control Assembly

#### 1-23 Test Tapes, Audio Signal Alignment

The audio signal alignment tapes are used as an alternative to the flux loop in reproduce equalization adjustments. See paragraph 5-30.

#### 1-24 SPECIFICATIONS

Specifications for the ATR-116/124 Recorder/Reproducer are given in Table 1-4. All specifications are subject to change without notice or obligation.

Table 1-4. Specifications

Tape Widths	Reel Size
1 in. 8 trk 2 in. 16 and 24 trk	5 in.—16 in.
Tape Speeds	Reel Type
7.5 in/s (19.05 cm/s) 15 in/s (38.1 cm/s) 30 in/s (76.2 cm/s)	NAB
Inputs	
Balanced, floating input impedance:	>20 KΩ, resistive, 5 Hz-20 kHz
Input level:	To produce 0 VU REFER- ENCE level: 0 dBm minimum, +16 dBm maxi- mum. Electronics clip level, including record amplifier at mid-frequency: 26 dB above system operating (0 VU) level.
Outputs	
Balanced, floating output impedance:	<50Ω, 5 Hz-20kHz
Maximum balanced output level:	With 200Ω load: +28 dBm.
Preset output level:	With 600Ω load: +4 dBm. Line output level is adjustable over a range of +12 dBm to -2 dBm
Metering:	VU meters whose ballistics conform only approximately to ASA standards.

Table 1-4. Specifications (Continued)

#### Equalization

Any of four selectable EQs (equalizers) may be assigned to any tape speed. These four EQs are then automatically switched with transport speed switch. Each selected EQ provides equalization adjustable over the range of AES/NAB/IEC/CCIR standards.

#### Overall Frequency Response

Speed	Ref. Freq.	Within ±.75 dB		Ref. Level* (0 dB is operating level)
30 in/s (76.2 cm/s)	1 kHz	200 Hz-20 kHz	40 Hz-30 kHz	0
15 in/s (38.1 cm/s)	1 kHz	100 Hz-15 kHz	25 Hz-20 kHz	. 0
7.5 in/s (19.05 cm/s)	1 kHz	100 Hz-10 kHz	25 Hz-15 kHz	-10 dB

<sup>\*</sup>Operating level is 370 nWb/m at 700 Hz for Ampex 456 tape and 260 nWb/mon at 700 Hz for Ampex 406/407 tape.

#### Signal-to-Noise Ratio

Overall signal-to-noise ratio at 7.5 in/s—30 in/s is measured with respect to a record level of 1040 nWb/m (9 dB above an operating level of 370 nWb/m) when using Ampex 456 tape or direct equivalent. At 1040 nWb/m mid-frequency, third harmonic distortion is less than 3%.

Tape Speed and Equalization	Track Format	30 Hz-18 kHz Unweighted	ANSI "A" Weighted	IEC/CCIR Reg 468 Weighted
30 in/s AES	16	72	76	68
	24	69	73	65
15 in/s IEC/CCIR	16	70	74	66
	24	67	71	63
15 in/s (38.1 cm/s) NAB	16	69	73	65
	24	66	71	62
7.5 in/s (19.05 cm/s)	16	71	74	64
NAB	24	68	71	61
7.5 in/s (19.05 cm/s) IEC/CCIR	16	68	71	63
	24	65	68	60

#### Table 1-4. Specifications (Continued)

#### System Distortion (7-1/2 in/s-30 in/s)

Overall record/reproduce distortion (using Ampex 456 tape or direct equivalent)

Even-order distortion:

<0.1% for a 1-kHz signal recorded at 370 nWb/m.

Third harmonic distortion at 1 kHz:

<0.3% at recorded flux level of

370 nWb/m (0 vu).

<3.0% at recorded flux level of 1040 nWb/m (+9 vu).

SMPTE intermodulation distortion:

<3% of recorded flux level of 740 nWb/m (+6 vu) for IEC/AES

equalizations.

<4% of recorded flux level of 740 nWb/m (+6 vu) for NAB

equalizations.

System electronics distortion, including record amplifier, reproduce amplifier and input/output circuitry, at any level up to 20 dB above operating level at mid-frequency, is <0.03% total harmonic distortion and <0.05% SMPTE intermodulation distortion.

#### Crosstalk

Crosstalk is measured by simultaneously placing the channel under test and an adjacent channel in record mode. The adjacent channel is fed with an operating level signal, the channel under test has its input shorted. The residual signal on the reproduced output of the channel under test relative to operating level is less than 50 dB, 100 Hz—12 kHz at 15 in/s.

#### Erase Depth

Using Ampex 456 tape or direct equivalent, at any wavelength shorter than 30 mils (500 Hz (d 15 in/s) recorded 6 dB above system operating level: 85 dB minimum.

Erase Frequency:

144 kHz

Bias Frequency:

324 kHz

(Both bias and erase frequencies are derived from master crystal oscillator)

Table 1-4. Specifications (Continued)

#### Speed Accuracy

Using 1.0 - 1.5 mil base film thickness tape.

Absolute speed accuracy:

±0.03%

Speed variation from beginning

to end of reel:

0.02% maximum

#### Flutter and Wow:

Speed	ANSI S 4.3/DIN 45507 Peak Weighted	ANSI/DIN Peak Unweighted	NAB RMS Unweighted
7.5 in/s (19.05 cm/s)	±0.05%	±0.12%	0.06%
15 in/s (38.1 cm/s)	±0.03%	±0.08%	0.04%
30 in/s (76.2 cm/s)	±0.03%	±0.08%	0.03%

#### Start Time (10-1/2 in. reel)

Speed:	Time to attain flutter specification:
7.5 in/s	200 ms
15 in/s	300 ms
30 in/s	500 ms

#### Stop Time (10-1/2 reel)

5.0s from wind modes

0.7s maximum from play mode (30 in/s, 76.2 cm/s)

#### **Rewind Time**

Normal fast wind modes:

120s for 2400 ft (731.52m)

reel.

#### **Electronic Tape Timer**

Tape driven; reads in hours, minutes, and seconds (option: minutes, seconds, and tenths of seconds)

#### Heads

Record/Repro: Metal with adjustable azimuth and racking

Erase: ferrite with adjustable racking

24 trk 2 in. 16 trk 2 in. 8 trk 1 in.

Table 1-4. Specifications (Continued)

Size

Width Depth 34.8 in. 32.2 in.

Height

49.5 in.

Weight

800 lbs

Power Line Requirements

90-115, 110-135, 180-230, 220-270 Vac, 50/60 Hz

**Power Consumption** 

1.5 kVA avg

**Environmental Operating Specifications** 

Temperature:

10°-40° C (50°-104° F)

Humidity:

20%-80%, noncondensing

# SECTION 2 INSTALLATION

#### 2-1 INTRODUCTION

This section of the manual provides information about the ATR-116/124 in regard to the following:

- Unpacking and inspection.
- Choosing the installation site.
- Equipment connectors and cabling.
- Initial adjustments.
- Initial checkout procedure.
- · Factory-shipped operational configuration.
- · Procedure for checking operating level.

#### 2-2 SITE SELECTION

The area chosen for operation of the recorder/reproducer should be adequately ventilated and free of vibration. Surrounding air should be dust-free with a temperature range within 50° to 104°F (10° to 40°C) and humidity within 20% to 80% (noncondensing). The area should not be close to any strong electromagnetic fields. Common sources of interference are nearby high current ac power lines, heavy-duty transformers, elevator motors, and radio and television transmitting equipment.

When installing the equipment allow sufficient space at the top, bottom, and rear of the unit to permit flow of cooling air. Refer to Figure 2-1 for spacing requirements of the ATR-116/124.

#### 2-3 UNPACKING

Upon receipt, examine the shipping crate for any signs of damage. Unpack and inspect the equipment for physical damage. Retain the shipping container. Check the packing list to determine that all items have been received. Immediately report any damages to the Ampex representative and the transportation company.

#### 2-4 POWER REQUIREMENTS

The ATR-116/124 requires 115/230V at 50/60 Hz (nominal). Power is connected by a grounding-type plug.

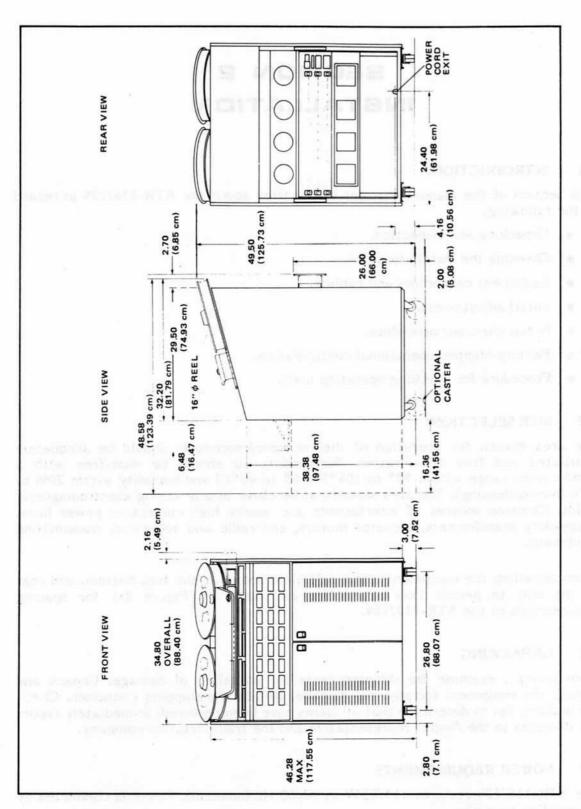


Figure 2-1. ATR-116/124 Recorder/Reproducer Dimensions

#### WARNING

ENSURE THAT THE POWER PLUG IS PROPERLY GROUNDED BY MEANS OF THE GROUND PRONG.

Determine the line input voltage and strap the power transformer according to Figure 2-2 to accommodate the input line voltage. Access to the power transformer is obtained by removing the bottom cover panel on the rear of the unit (Figure 1-8).

#### WARNING

DISCONNECT LINE VOLTAGE BY UNPLUGGING THE POWER CORD BEFORE MAKING ANY ADJUSTMENTS ON THE POWER TRANSFORMER. ALL EXPOSED TERMINALS HAVE LINE VOLTAGE PRESENT WHEN POWER IS APPLIED.

#### 2-5 CABLE CONNECTIONS

Audio signals are connected to and from the ATR-116/124 by connectors on the I/O panel shown in Figure 2-3. The connectors are three-conductor XLR type. Female connectors are used for the input signals and male connectors are used for the output signals. The mating plugs are user-supplied, XLR type, and should be used with shielded-pair audio cable to provide input and output connections. Wire the mating plugs as shown in Figure 2-4 according to the required usage.

The I/O panel also contains an accessory connector, a remote control connector, a noise reduction trigger connector, and time code connectors. Table 2-1 lists the pin assignments for the remote connector. Table 2-2 lists the pin assignments for the accessory connector. Table 2-3 lists the pin assignments for the noise reduction trigger connector. Table 2-4 is a listing of the connector pin-out mnemonics and identifies the various connector output functions. The time code connectors are for future use and are not connected at this time.

#### 2-6 INITIAL CIRCUIT BOARD ADJUSTMENTS

Alternate positioning of switches and jumpers on some of the circuit boards of the recorder may be required to provide selective functions or operational requirements. Table 2-5 lists selective functions and operations which may require alternate positioning of switches and jumpers on the circuit boards affected.

#### 2-7 INITIAL CHECKOUT PROCEDURES

Use these instructions to verify that the system is operating correctly. See Section 3 for operating instructions as necessary. Proceed as follows:

#### CAUTION

BEFORE CONNECTING AC POWER, REFER TO INSTRUCTIONS GIVEN IN PARAGRAPH 2-4 REGARDING POWER REQUIREMENTS.

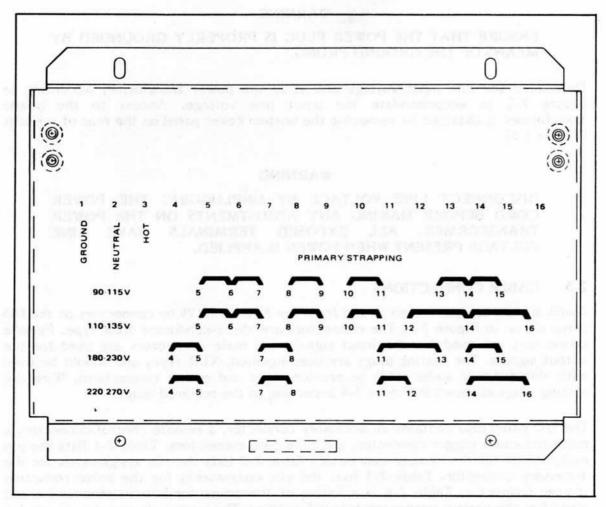


Figure 2-2. Power Supply Strapping

- STEP 1 Connect ac power cord to a suitable power source.
- STEP 2 Turn circuit breaker on and push ON. All safe and repro indicators light, stop indicator lights, and tape timer display indicates 0:00:00. Once signal system is set up for operation (see Section 3 of this manual), the stay-alive battery power supply maintains operator setup in memory. Thereafter, setting power switch to ON does not result in all safe and repro indicators lighting, but rather the operator-selected setup is displayed on signal system matrix.
- STEP 3 Set tape speed pushbutton to desired tape speed.
- STEP 4 Install reel of tape on supply turntable and an empty reel on take-up turntable.
- STEP 5 Thread tape on transport see paragraph 3-3) and activate the reel servos by tensioning the tape.

#### Note

The reel servos cannot be activated until after the wakeup period has ended, i.e., after the panel LEDs stop flashing.

#### STEP 6 Check tape transport operation and control circuitry as follows:

- a. Press PLAY. Transport operates at speed selected and play indicators light. (Top of play indicator lights on play command; bottom indicator lights when play speed has stabilized.)
- b. Press STOP. Tape stops and stop indicator lights. (Top of the stop indicator lights on stop command; bottom of the stop indicator lights when tape motion has stopped.)
- c. Press FAST FORWARD. Transport enters fast forward mode and fast forward indicator lights.
- d. Press REWIND. Transport enters rewind mode and rewind indicator lights. Press STOP.
- e. Turn capstan edit knob by hand in one direction and then the other. Tape moves from reel to reel under reel-servo control; tape timer display will increase or decrease accordingly.
- f. Press SERVO DISARM. The servo disarm lamp lights and tape tension will relax.
- g. Turn capstan edit knob by hand in one direction and then the other. Tape will not move from reel-to-reel under reel-servo control.
- h. Retension tape to activate servos. Press STOP.
- Depress FAST FORWARD or REWIND. Press and hold LIFT DEFEAT. Lifters retract and tape is in contact with tape heads.
- Press PLAY. Press and hold LIFT DEFEAT. Tape is lifted from heads. Press STOP.

#### STEP 7. Check signal system control circuitry as follows:

- a. Press READY. Press a channel select pushbutton. The channel-ready indicator (yellow) lights. Repeat this step for all channels as applicable.
- b. Press RECORD and PLAY simultaneously. Ready indicator will go out; the channel record indicator (red) and the record pushbutton indicator (red) lights. Panel meter corresponding to channel selectedis backlit in red.
- c. Press STOP. Channel record indicator and master record indicator go out and ready indicator lights. Panel meter corresponding to channel selected is no longer backlit in red.
- d. Press SAFE. Press a channel-select pushbutton. Safe indicator lights and ready indicator goes out. Repeat this step for all channels as applicable.

- e. Press PLAY and RECORD simultaneously. Channel record indicator (red) and record pushbutton indicator do not illuminate. (This occurs only if no channel is in ready.)
- f. Press SYNC. Press a channel select pushbutton. Sync indicator lights. Repeat this step for all channels as applicable.
- g. Press REPRO. Press a channel select membrane switch. Repro indicator lights and sync indicator goes out. Repeat this step for all channels as applicable.
- h. Depress INPUT. Press a channel select pushbutton. Input indicator lights illuminate and repro indicator goes out. Repeat this step for all channels as applicable.

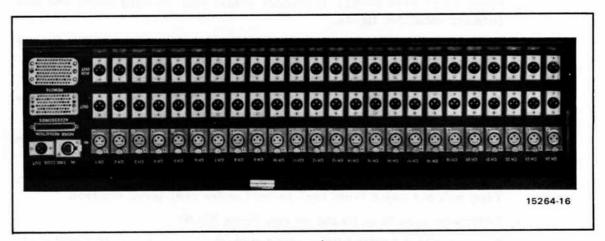


Figure 2-3. I/O Panel

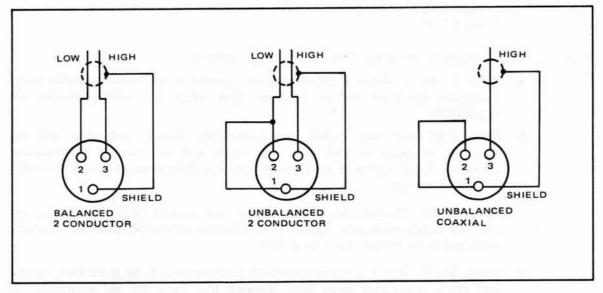


Figure 2-4. Input/Output Connector Wiring

Table 2-1. ATR-116/124 Remote Connector Pin Designations

Wire No.	Terminal No.	Function	Wire No.	Terminal No.	Function
1	Α	GND	44	у	SP
	В	GND	45	z	TGND
3	С	+LV	46	AA	TRB
2 3 4 5 6 7 8 9	D	+LV	47	AB	CSB
5	E	SP	48	AC	SIGN
6	F	SP	49	AD	BCDA
7	Н	SP	50	AE	BCDB
8	J	SVI	51	AF	BCDC
9	K	SP1	52	AH	BCDD
10	L	SP2	53	AJ	DSA
11	М	SP3	54	AK	DSB
12	N	SP4	55	AL	DSC
13	P	SP5	56	AM	SP
14	R	SP6	57	AM	R0
15	S	SP7	58	AP	RI
16	T	SP8	59	AR	R2
17	U	SCHB	60	AS	R3
18	V	SCHC	61	AT	R4
19	w	CUDC	62	AU	R5
20	X	SPS	63	AV	R6
21		STB	64	AW	R7
22	Y Z	STI	65	AX	DOA0
23	a	MTI	66	AY	DOAL
24	b	FFB	67	AZ	DOA2
25	c	FFI	68	BA	DOA3
26	d	RWB	69	BB	DOB0
27	f	RWI	70	BC	DOB1
28	No. 10 Page 1	SHB	71	BD	DOB2
29	g h	PLB	72	BE	DOB3
30		PLI	73	BF	DSL0
31		LKI	74	BH	DSL1
32	k	RCC	75	BJ	DSL2
33	m	RCS	76	BK	DSL3
34		RCB			
35	n		77	BL	SWV
36	P	RCI	78	BM	SWW
37	q	ERSI	79	BN	SWX
	r	RHS	80	BP	SWY
38	S	RHB	81	BR	MPGND
39	t	RHI	82	BS	SP
40	u	RHLI	83	BT	SP
41	V	RHC	84	BU	SP
42	w	LDB	85	BV	RPDL
43	x	SP	86	BW	RPDH

Table 2-1. ATR-116/124 Remote Connector Pin Designations (Continued)

Wire No.	Terminal No.	Function	Wire No.	Terminal No.	Function
87	BX	RCDL	96	СН	WUL
88	BY	RCDH	97	CJ	SP
89	BZ	ART	98	CK	SP
90	CA	ARC	99	CL	SP
91	СВ	ARH	100	CM	SP
92	CC	SHVN	101	CN	SP
93	CD	SHGND	102	CP	SP
94	CE	SHS	103	CR	NC
95	CF	SHVP	104	CS	SHIELD

Table 2-2. ATR-116/124 Accessory Connector Pin Designations

Wire No.	Terminal No.	Function	Wire No.	Terminal No.	Function
1	1	GND	28	32	PLC ·
	4	GND	29	30	LKD
3		SP	30	33	SP
2 3 4 5	2 5 3	SP	31	34	RCS
5	3	+8V	32	37	RCC
6	7	+8V	33	35	ERS
6	8	-15V	34	38	RHS
8	12	+15V	35	36	RHC
9	10	-CV	36	39	LDB
10	13	+CV	37	40	SSA
11	11	SP	38	43	SSB
12	14	SP	39	41	SP
13	15	SVO	40	44	XTL
14	18	SP	- 41	42	TPC
15	16	SP	42	45	TPR
16	20	SP	43	46	EXC
17	17	SP	44	49	EXR
18	21	SCHC	45	47	SP
19	22	SP	46	50	TTAC
20	25	STB	47	48	TDR
21	23	STC	48	51	CTAC
22	26	MTS	49	52	SP
23	24	FFB	50	55	TGND
24	27	RWB	51	53	SIGN
25	28	SHB	52	56	BCDA
26	31	SHC	53	54	BCDB
27	29	PLB	54	57	BCDC

Table 2-2. ATR-116/124 Accessory Connector Pin Designations (Continued)

Wire No.	Terminal No.	Function	Wire No.	Terminal No.	Function
55	58	BCDD			
56	62	DSA	66	72	ARC
57	59	DSB	67	73	ARH
58	63	DSC	68	76	SHVN
59	60	SP	69	74	SHGND
60	64	SP	70	77	SHS
61	65	RPDL	71	75	SHVP
62	70	RPDH	72	78	WUL
63	66	RCDL	73	79	SP
64	71	RCDH	74	80	SP
65	67	ART	75	82	SP

Table 2-3. ATR-116/124 Noise Reduction Trigger (NRT) Connector Pin Designations

Wire No.	Terminal No.	Function	Origin No.	Wire No.	Terminal No.	Function	Origin No.
	- b 1-6-		CB1		On-	HEAD GROSS	
1	1	CH4 NRT	P29	16	27	CHI6 NRT	P29
2	20	CH5 NRT	P29	17	9	CHIO NRT	P29
3	2	CH6 NRT	P29	18	28	CHII NRT	P29
4	21	CH7 NRT	P29	19	10	CONT GND	P29
5	3	CHI NRT	P29	20	29	+15V	P29
6	22	CH8 NRT	P29				
7	4	CH2 NRT	P29			Spirm Bull	CB3
8	23	CH3 NRT	P29	21	n Halker	C1100 110 m	15 = 15 L
9	5	CONT GND	P29	21	11	CH20 NRT	P29
10	24	+15V	P29	22	30	CH21 NRT	P29
		a addition	1345	23	12	CH22 NRT	P29
		a military	CB2	24	31	CH23 NRT	P29
11		CHIZNET	D20	25	13	CH17 NRT	P29
26.1627	6	CH12 NRT	P29	26	32	CH24 NRT	P29
12	25	CH13 NRT	P29	27	14	CHI8 NRT	P29
13	20	CHI4 NRT	P29	28	33	CHI9 NRT	P29
14	26	CH15 NRT	P29	29	15	CONT GND	P29
15	8	CH9 NRT	P29	30	34	+15V	P29

Table 2-4. ATR-116/124 Mnemonics for System Commands and Status Signals

Code	Meaning	Code	Meaning
ARC	Auto record (panel	ARH	Auto rehearse (panel CPU interrupt)CPU interrupt)

Table 2-4. ATR-116/124 Mnemonics for System Commands and Status Signals (Continued)

Code	Meaning	Code	Meaning
ART	Auto rec/reh terminate	RCI	Upper record indicator
	(panel CPU interrupt)	RCS	Record switch (source
BCDAD	Tape time display code	RCB	of except when inter-
BCS	Bias command status		rupted by MPSTC edit
CSB	Cue store button		pre-roll)
CTAC	Capstan tach output	RHB	Rehearse button (see
CUDC	Cued command	383	RHS)
DOA03	MPSTC display code	RHC	Rehearse command
DOB03	MPSTC display code	RHI	Rehearse indicator
DSAC	Tape time display code	RHLI	Rehearse lower
DSL03	MPSTC display code	1 7 87	indicator
EBS	Erase bias status	RHS	Rehearse switch
ERS	Electronics record	Contracted to	(source of RHB except
	status		when interrupted by
ERSI	Electronics record	I Courts II	MPSTC edit preroll)
101/2	status indicator	RPDH	Remote panel data-high
EXC	External control	0.00	(audio setup)
	(capstan ref)	RPDL	Remote panel data-low
EXR	External reference		(Audio setup)
	(9600 Hz input)	RWB	Rewind button
FFB	Fast forward button	RWI	Rewind indicator
FFI	Fast forward indicator	SCHB	Search button
GND	Ground	SCHC	Search command
ISL	Illegal speed line	SDB	Servo disarm button
LDB	Lift defeat button	SHB	Shuttle button
LKD	Locked (capstan servo)		(command)
LKI	Locked indicator	SHC	Shuttle command
1000	(capstan servo)	SHGND	Shuttle ground
MPGND	MPSTC ground	SHS	Shuttle sense
MTI	Motion sense indicator	SHV	Shuttle voltage
MTS	Motion sense	SIGN	Tape time sign
NC	No connection	SP	Spare
NRT	Noise reduction trigger	SP1 8	Spare lines for future
PLB	Play button		switches
PLC	Play command	SSA,B,C	Speed select (coded
PLI	Play indicator		lines)
R07	MPSTC display code	STB	Stop button
RCB	Record button (see RCS)	STC	Stop command
RCC	Record command	STI	Stop indicator
RCDH	Remote control-bay	SVA	Servos armed
	data—high (audio setup)	SVI	Servo disarmed
RCDL	Remote-control bay	Lyn	indicator
	data—low (audio setup)		

Table 2-4. ATR-116/124 Mnemonics for System Commands and Status Signals (Continued)

Code	Meaning	Code	Meaning
SVO SWVY	Servo on command MPSTC display code	TRB TTAC	Tape timer reset buttor Tape timer tach
TDR	True direction of tape	VSC WUL	VSO control Wake-up line
TGND	Tape timer ground	XTL	Crystal ref (9600 Hz)
TLM	Torque limit	±CV	Control supply voltage
TPC	Tape control (capstan ref)	+LV	Lamp supply voltage (variable)
TPR	Tape reference (9600 Hz input)		

Table 2-5. PWA Jumper and Switch Connections-Initial Adjustments

PWA	Jumper Switch	Fig. No.	Function
Capstan Servo/ Transport Control	Play-off/stop (S1)	2-5	Selects stop (up) or play-off (down) tape feature at tape end.
Control	Service mode (S2)	2-5	In service position (down), maintains capstan servo operation regardless of presence or absence of tape.
	Play direction rev/ fwd (S3)	2-5	Reverses normal play direction of tape in REV (down) position.
Main CPU	Baud rate selector (S1)	2-6	Selects baud rate for PWA UART by means of wire link.
Main CPU	Power lock-out (J1)	2-6	In A-B jumper position, battery circuit for RAM stay- alive function is operative; are jumper position for test purposes only.
Panel CPU	Baud rate selector	2-7	Selects baud rate for PWA UART by means of a wire link.
Search-to- Cue	LED display (J1)	2-8	In A-D jumper position, tape timer display corresponds to

Table 2-5. PWA Jumper and Switch Connections—Initial Adjustments (Continued)

PWA	Jumper Switch	Fig. No.	Function
Search-to- Cue (Continued)	Tops the first Tags the Tags Tags Tags Tags Tags Tags Tags Tags		placarding (hours, minutes, seconds); in B-D position, shows minutes, seconds, and tenths of seconds; C-D position is a test position.
Audio Test	16/24 channel select (J3)	2-9	Jumpered between A-C for 16- channel rollover of 2-digit channel display on audio test PWA; jumpered between B-C for 24-channel rollover.
ATOSOUTA	Aux bus display/Chl (J4)	Later (March	Determines whether output of channel I only or channel indicated on channel display of Audio Test PWA is present on aux connector.
Audio	RLFB (J101)	2-10	B-C position inhibits NAB record low-frequency boost from being selected for individual channel.
	Record inhibit (J201)		B-C position inhibits record capability for individual channel.

#### 2-8 FACTORY SHIPPED OPERATIONAL CONFIGURATION

The basic recorder/reproducer is capable of operating at tape speeds of 7.5 in/s, 15 in/s, and 30 in/s (19.05 cm/s, 38.1 cm/s, and 76.2 cm/s) in the NAB, IEC, or AES equalization standard. The recorder/reproducer is shipped from the factory in the operational configuration given in Table 2-6. Some applications of the recorder/reproducer require a configuration different from those established at the factory.

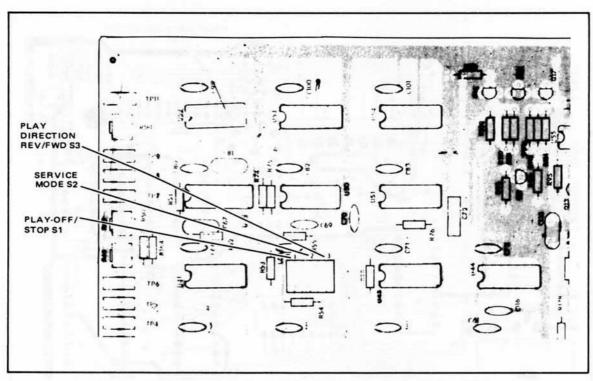


Figure 2-5. Capstan Servo/Transport Control PWA—Play Direction S1, S2 and S3—Location

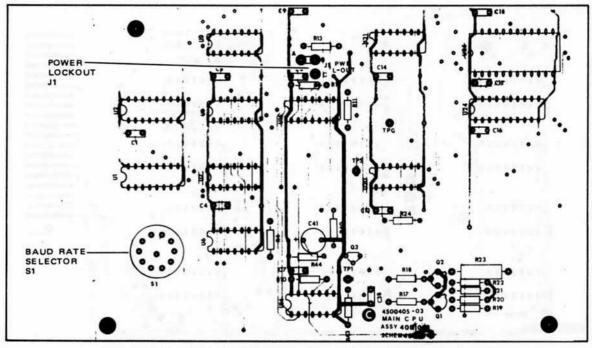


Figure 2-6. Main CPU PWA—Baud Rate Selector S1 and Power Lock-out Jumper J1—Location

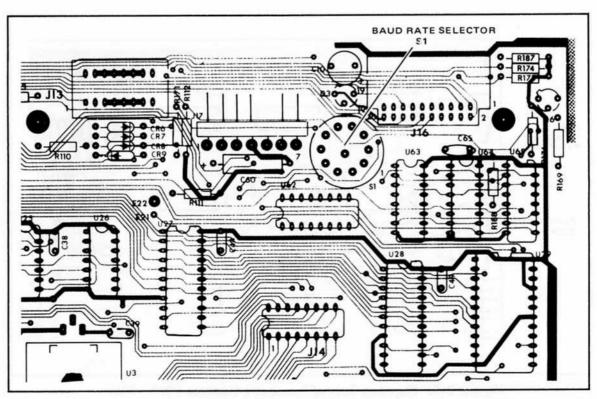


Figure 2-7. Panel CPU PWA-Baud Rate Selector S1-Location

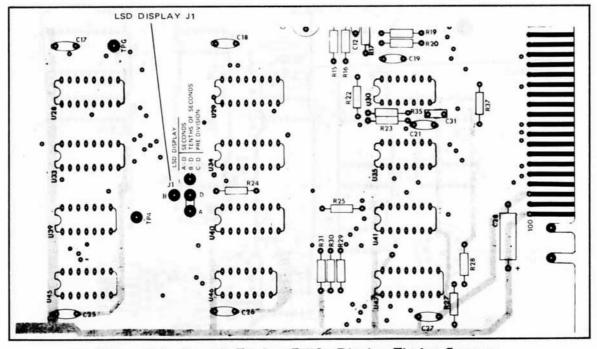


Figure 2-8. Search-To-Cue PWA—Display Timing Jumper J1—Location

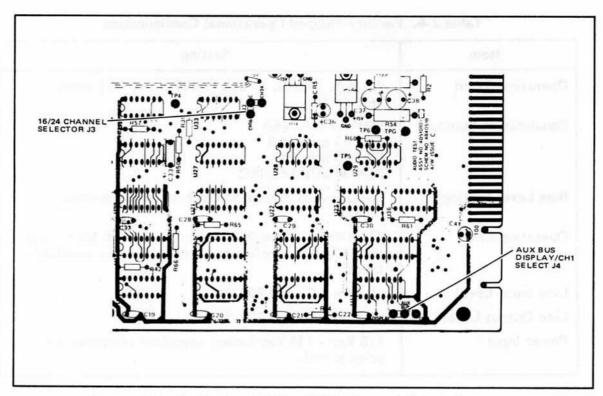


Figure 2-9. Audio Test PWA-16/24 Channel Select Jumper

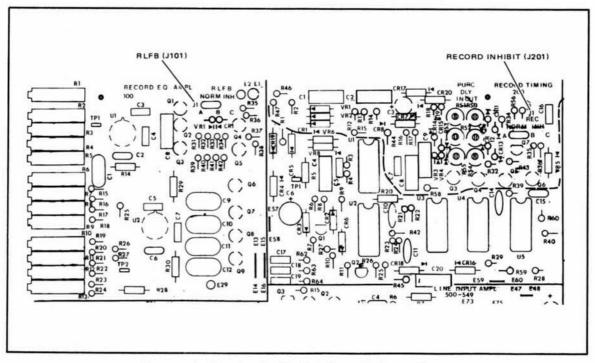


Figure 2-10. Audio PWA-Jumper Locations

Table 2-6. Factory-Shipped Operational Configuration

Item	Setting
Operating Speed	7.5 in/s, 15 in/s, 30 in/s (19.05 cm/s, 38.1 cm/s, 76.2 cm/s).
Equalization Standard	EQ1 7.5 in/s NAB EQ2 15 in/s NAB EQ3 15 in/s IEC EQ4 30 in/s AES/IEC
Bias Level Setting	For use with Ampex 456 high-output, low-noise tape.
Operating Level	370 nWb/m = 0 vu @ 700 Hz: This is 6 dB higher than the 185 nWb/m reference level of Ampex standard tapes.
Line Input Level	+4 dBm = 0 vu @ 700 Hz
Line Output Level	+4 dBm = 0 vu (d 700 Hz
Power Input	110 Vac - 135 Vac (unless specified otherwise on sales order).

# SECTION 3 OPERATION

#### 3-1 INTRODUCTION

This section of the manual provides information on locations and functions of the recorder/operating controls and indicators, a preoperational procedure, and operating instructions for the various modes of operation.

#### 3-2 CONTROLS AND INDICATORS

Tables 3-1 and 3-2 list the transport controls and indicators that are located on the machine and setup panels. Table 3-3 lists the signal controls and indicators that are located on the setup panel. Table 3-4 lists the secondary controls that are located on the secondary control panel.

Figure 3-1 shows the location of controls for main power/circuit breaker, lamp adjust, manual adjust. Figure 3-2 shows placement of capstan edit control and speaker volume control.

The MAIN POWER switch connects the ATR-116/124 to the power line in the ON position and it disconnects from the power line in the OFF position (this switch does not affect the memory battery power supply operation). The MAIN POWER switch is also the main circuit breaker reset.

The lamp-adjust control adjusts incandescent indicator lamp brightness to operator-determined level.

The capstan edit control is used when tape is stopped and the reel servos are armed. Turning this control by hand in either direction moves tape from reel-to-reel under reel servo control.

The speaker volume control adjusts the keyboard tone volume to an operatordetermined level. Turning the volume all the way down mutes the tone.

Table 3-1. Machine Control Panel, Transport Controls and Indicators

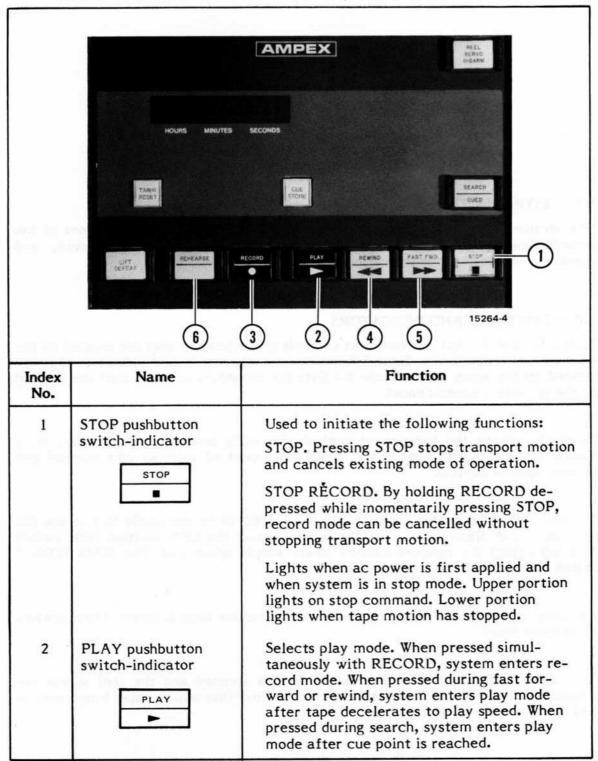


Table 3-1. Machine Control Panel, Transport Controls and Indicators (Continued)

Index No.	Name	Function
2	PLAY pushbutton switch-indicator (Continued)	Upper indicator lights when play is selected. Lower indicator lights when the capstan servo is locked (green).
3	RECORD pushbutton switch-indicator	Simultaneously pressing RECORD and PLAY initiates record mode for those channels assigned to ready mode. Play mode can be entered from record mode without interrupting tape motion by holding RECORD depressed while momentarily pressing STOP.
		Upper indicator lights on record command. Lower indicator lights in conjunction with PLAY indicator when any channel is recording (red). If servo lock is lost, record mode is cancelled.
4	REWIND pushbutton switch-indicator	Selects rewind mode. The whole indicator lights (white) when rewind mode is entered. Operates in parallel with variable speed shuttle control.
5	FAST FORWARD pushbutton switch-indicator	Selects fast forward mode. The whole indicator lights (white) when fast forward mode is entered. Operates in parallel with variable speed shuttle control.
6	REHEARSE pushbutton switch-indicator	When selected (during play mode only), monitoring is changed over to record setup without actually recording on tape. Rehearse is terminated by entering stop mode or pressing PLAY during rehearse mode. The whole indicator lights (white) when rehearse is selected.

Table 3-1. Machine Control Panel, Transport Controls and Indicators (Continued)

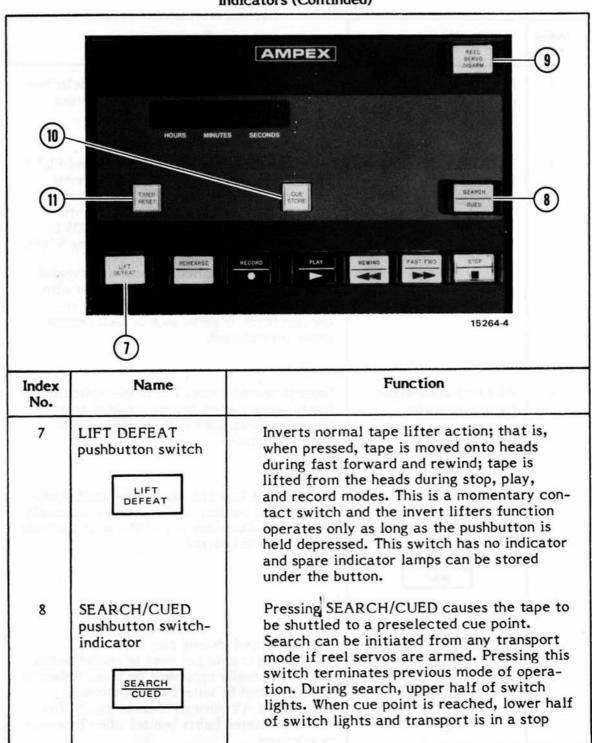


Table 3-1. Machine Control Panel, Transport Controls and Indicators (Continued)

Index No.	Name	Function
8	SEARCH/CUED pushbutton switch- indicator (Continued)	mode. Play mode can be entered at end of search by pressing PLAY during search interval.
9	REEL SERVO DISARM pushbutton switch-indicator	Disarms reel servos. Can only be selected during stop mode. Indicator lights (yellow) when actuated. Indicator stays lit when servo is disarmed. This switch does not function on the remote control panel. The remote control panel reel servo disarm reel servo disarm indicator functions, however, as an indicator only.
		(a) (a) " " " "
10	CUE STORE pushbutton switch	Pressing this pushbutton switch stores the immediate tape location cue point to which tape is to be shuttled when the search pushbutton switch is pressed.
11	TIMER RESET pushbutton switch	Resets tape timer to 0:00:00. Also used in conjunction with SEARCH/CUED pushbuttor during search-to-cue looping setup (paragraph 3-19).

Table 3-2. Setup Panel, Transport Controls and Indicators

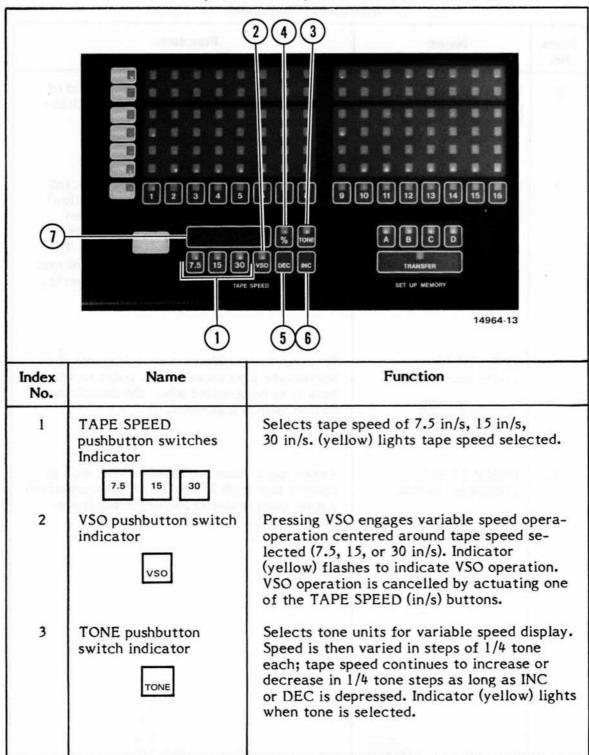
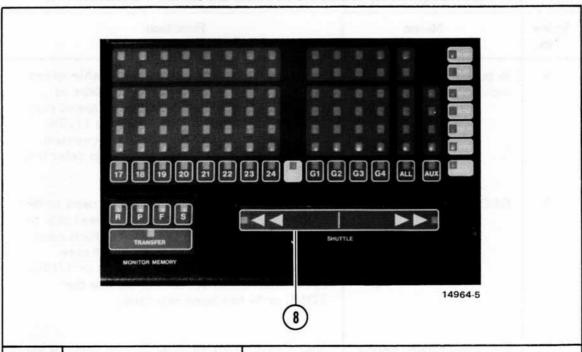


Table 3-2. Setup Panel, Transport Controls and Indicators (Continued)

Index No.	Name	Function
4	% pushbutton switch indicator	Selects percentage units for variable speed display. Speed is then varied in steps of approximately 1/10% each; tape speed continues to increase or decreases in 1/10% steps as long as INC or DEC is depressed. Indicator (yellow) lights when % is selected.
5	DEC pushbutton switch	Speed decrement switch. Can be used to decrease tape speed by pressing repeatedly to step manually or by holding, in which case the speed decreases at a constant rate. Speed change is in 1/4-tone steps or 1/10% of nominal steps depending on whether TONE or % has been selected.
6	INC pushbutton switch	Speed increment switch. Can be used to increase tape speed by pressing repeatedly to step manually or by holding down, in which case the speed increases at a constant rate. Speed change is in 1/4-tone steps or 1/10% of nominal speed steps depending on whether TONE or % has been selected.
7	TAPE SPEED display	The 4-digit display indicates the VSO speed offset in either % or tones as selected. Actuating a nominal speed selector cancels VSO operation. This does not return the display to nominal speed; rather, the display continues to indicate VSO speed. The VSO INC or DEC control may be used with the display to set up VSO speed while the transport is operating at nominal speed.  The VSO display can be returned to nominal by either manual use of the INC or DEC switches, or by pressing the VSO test button on the handle of the VSO PWA in the control

Table 3-2. Setup Panel, Transport Controls and Indicators



Index No.	Name	Function
8	Shuttle variable speed control, indicator	Selects variable forward and rewind shuttle. Speed is controlled by pressing control at center position for zero speed; at the outer position for maximum speed. Speed is variable at any point between zero and maximum and is latched at the point last depressed. It is, therefore, unnecessary to continue depressing control once desired speed is selected. Operates in parallel with REWIND and FAST FORWARD pushbutton switches. Indicators (yellow) light to indicate direction when selected.

Table 3-3. Setup Panel, Signal System Controls and Indicators

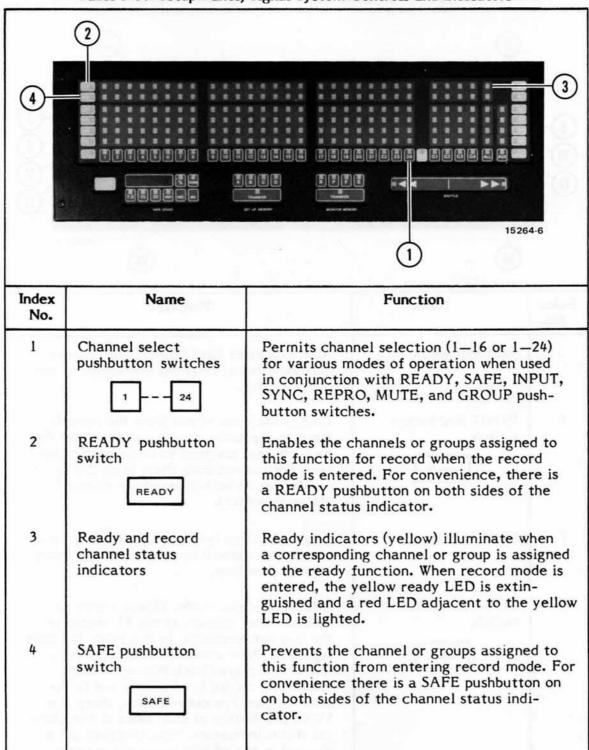


Table 3-3. Setup Panel, Signal System Controls and Indicators (Continued)

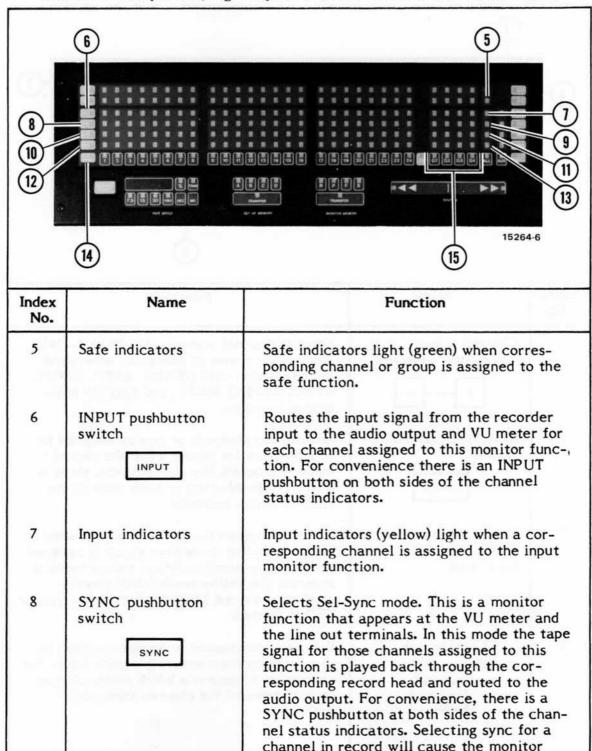


Table 3-3. Setup Panel, Signal System Controls and Indicators (Continued)

Index No.	Name	Function	
8	SYNC pushbutton switch (Continued)	for that channel to switch to input, then go into sync when the channel exits record.	
9	Sync indicators	Sync indicators lights (yellow) when a cor- responding channel is assigned to the sync monitor function.	
10	REPRO pushbutton switch	Connects signal reproduced by reproduce head to the VU meter and line output termminals for each channel assigned to this monitor function. For convenience there is a REPRO pushbutton at both sides of the channel status indicators.	
11	Repro indicators	Repro indicators light (yellow) when a cor- responding channel is assigned to the repro monitor function.	
12	MUTE pushbutton switch	In mute, each channel assigned to this monitor function has no line output or VU meter drive. For convenience there is a MUTE pushbutton at both sides of the channel status indicators. (Mute does not interrupt the record process, it only interrupts the monitoring process.	
13	Mute indicators	Mute indicators light (yellow) when a cor- responding channel is assigned to the mute monitor function.	
14	GROUP pushbutton switch	Attaches or detaches channels to or from group status. For convenience there is a GROUP pushbutton at both sides of the channel status indicators.	
15	Group assign/select pushbutton switches	In conjunction with channel select push- buttons, the GROUP pushbutton attaches channels to any of four desired groups. Each group (G1-G4) can then be set up as a single channel.	

Table 3-3. Setup Panel, Signal System Controls and Indicators (Continued)

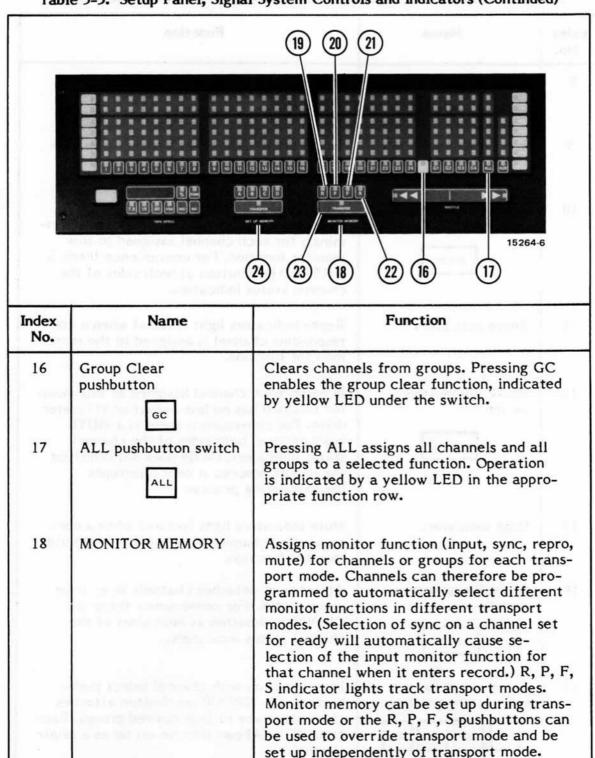


Table 3-3. Setup Panel, Signal System Controls and Indicators (Continued)

Index No.	Name	Function
19	R pushbutton switch- indicator	Monitor memory record mode. Allows programming of individual channel monitor functions during record mode. Indicator lights (yellow) when selected or in record mode.
20	P pushbutton switch-indicator	Monitor memory play mode. Allows pro- grainming of individual channel monitor functions to happen during play mode. In- dicator lights (yellow) when selected or in play mode.
21	F pushbutton switch-indicator	Monitor memory fast forward/rewind mode. Allows programming of individual channel monitor function during fast forward or rewind modes. Indicator lights (yellow) when selected or in fast forward or rewind mode.
22	S pushbutton switch indicator	Monitor memory stop mode. Allows programming of individual channel functions during stop mode. Indicator lights (yellow) when selected or in stop mode. Monitor memory tracking of transport modes can be disabled by pressing the S pushbutton switch while the S indicator is illuminated. Monitoring will remain in the S mode for all transport modes.
		Note R, P, F, S indicators flash if select- ed when the transport is not in the same mode.
23	TRANSFER pushbutton	Monitor Memory Transfer. Transfers the monitoring assignments of one mode of transport operation into another unaltered. Indicator flashes (yellow) after switch is pressed and until a monitor memory mode switch is pressed.
24	SET UP MEMORY	Stores four complete signal switching setups including all recording, monitoring, group and monitor memory functions.

Table 3-3. Setup Panel, Signal System Controls and Indicators (Continued)

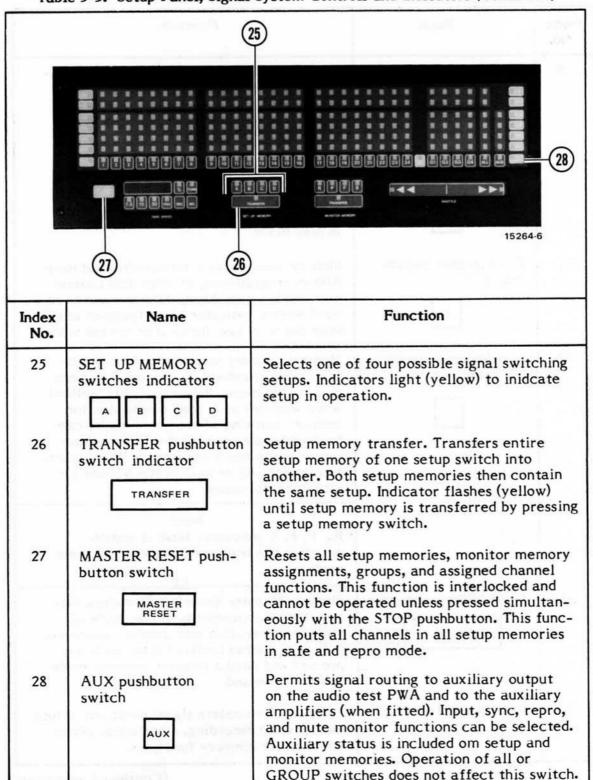
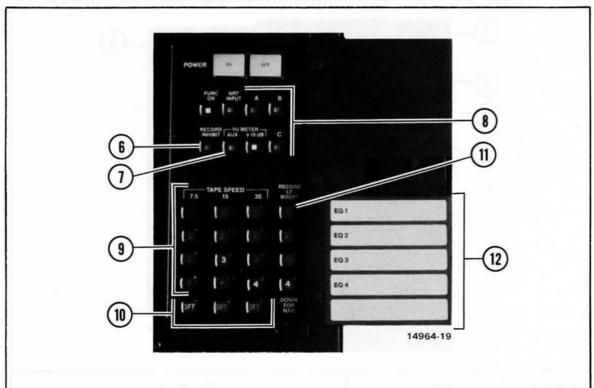


Table 3-4. Secondary Control Panel, Controls and Indicators

Index No.	Name	Function
-1	POWER ON switch- indicator	Controls power relay. When ON is selected, a green lamp indicates the machine is plugged in and power is applied to the machine.
2	POWER OFF switch- indicator	Turns power off. When selected, a red indicator lights to indicate stay-alive memory battery charger is operating, but system power is off.
3	PURC ON switch	When depressed, PURC circuitry is active.
4	RECORD INHIBIT switch	When depressed, the machine cannot record or rehearse.
5	NRT INPUT switch	When depressed the noise reduction trigger bus is activated in input as well as the record mode for cueing accessory noise reduction units. When not depressed, the bus is activated in record mode only.

Table 3-4. Secondary Control Panel, Controls and Indicators (Continued)



Index No.	Name	Function
6	VU METER AUX switch	Switches the VU meters from the main monitor output to the auxiliary monitor output when depressed.
7	VU METER +10 dB	When depressed, meter gain (not output) is boosted by +10 dB. This switch is for use with 7-1/2 in/s alignment tapes.
8	A, B, C	These pushbuttons are spares and perform no function on the machine as factory supplied.
9	TAPE SPEED equalization select pushbutton	Selects one of four factory-set equalization level and bias set-ups as follows (using Ampex 456 tape):
		EQ1 7.5 in/s NAB (370 nWb/m = 0 vu) EQ2 15 in/s NAB (370 nWb/m = 0 vu) EQ3 15 in/s IEC (370 nWb/m = 0 vu) EQ4 30 in/s AES/IEC (370 nWb/m = 0 vu)

Table 3-4. Secondary Control Panel, Controls and Indicators (Continued)

Index No.	Name	Function
		Note Other equalization and bias setups may be obtained through appropriate adjustments.
10	TAPE SPEED OFF (3)	When no equalization setup is assigned to a particular speed, OFF should be depressed for that speed. Machine does not operate in play or record if a speed for which OFF is selected is entered. Also, TAPE SPEED display will indicate ERRI (error 1).
11	RECORD LF BOOST	When depressed, pushbutton selected (1 of 4) assigns an NAB low-frequency record boost to equalization setup for which it is depressed. For example, pressing RECORD LF BOOST pushbutton no. 1 assigns an NAB low-frequency boost to equalization setup no. 1 for all channels.
12	Label	The operator may mark equalization setup specifications on this erasable surface. This allows identification of equalization setup corresponding to each row of pushbutton switches.

#### 3-3 PREOPERATING PROCEDURES

See Figure 3-3 and perform the following preoperational procedure.

- STEP 1 Clean and demagnetize components in tape path.
- STEP 2 Set POWER switch to ON. All SAFE and REPRO indicators light, tape timer indicates 0:00:00.

#### Note

Once signal system is set up for operation, the stay-alive battery power supply maintains operator setup in memory. Thereafter, setting power switch to ON does not result in all safe and reproindicators lighting, but rather the previous operator-selected setup is displayed on signal system matrix. To reset signal system, press STOP and MASTER RESET simultaneously.

STEP 3 Set speed select membrane switch to desired speed: 7.5 in/s, 15 in/s, 30 in/s.

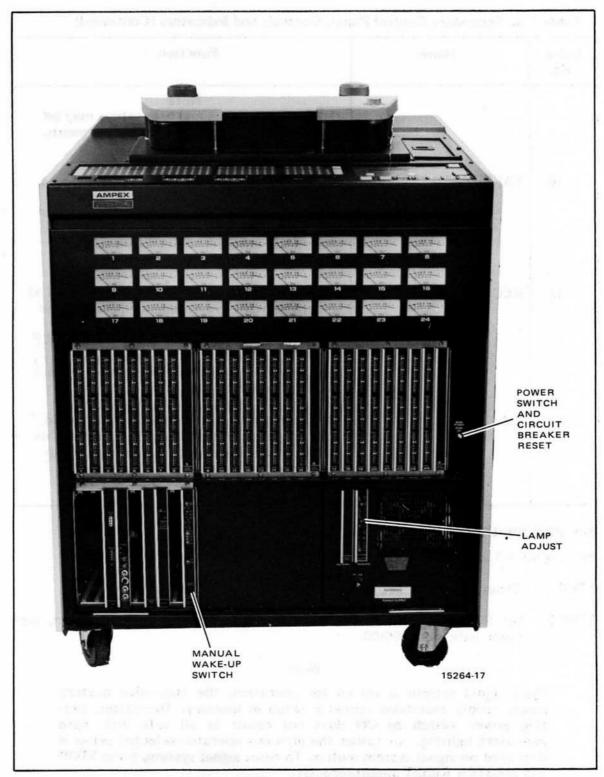


Figure 3-1. Power/Circuit Breaker, Lamp Adjust, and Manual Wakeup Switch Location

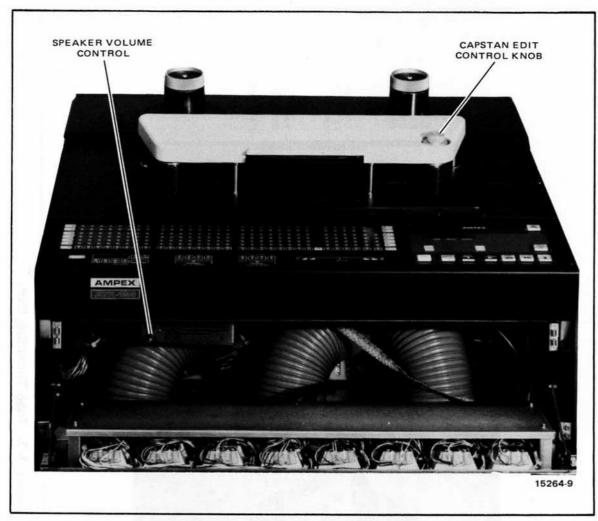


Figure 3-2. Capstan Edit, Speaker Volume Control Location

- STEP 4 Install a reel of tape on supply turntable and an empty reel on take-up turntable as shown in Figure 3-3. Reels up to 16 inches in diameter may be used. Reel size switching for different reels is not necessary.
- STEP 5 Open the head shield gate by pulling it away from heads.
- STEP 6 Lift the tape path cover.
- STEP 7 Thread tape on transport, as shown in Figure 3-3 and spool several turns of tape on to takeup side by hand-turning both supply and take-up reels in a counterclockwise direction.
- STEP 8 Turn reels to remove tape slack. Tighten until REEL SERVO DISARM indicator on machine control panel goes out. This arms reel servos in a torque-limited condition.

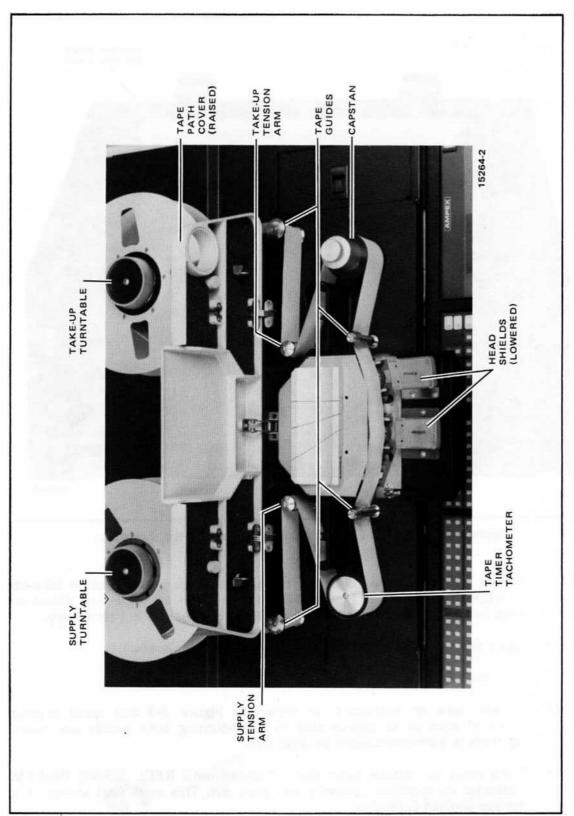


Figure 3-3. Tape Threading Path

#### CAUTION

DO NOT TOUCH THE TENSION SENSING ARMS WHEN RECORDER IS IN THE TAUT THREADED CONDITION. TO DO SO INTRODUCES A REEL SERVO ERROR THAT COULD CAUSE TAPE DAMAGE.

STEP 9 Close head shield gate and cover.

#### 3-4 OPERATING PROCEDURES

The following general information is applicable to all modes of operation:

- If the tape runs completely off the take-up or supply reel, the recorder is dynamically braked to a stop and the tape timer display freezes. Normally, the reel diameter measurement circuitry prevents the tape from running completely off the reel in shuttle by stopping tape motion. This feature can be overridden by holding the fast wind button down and tape can then run completely off the reel.
- For any given channel, selection of RECORD, READY, or SAFE mode may be made one at a time. Similarly, one of the four monitor functions (input, sync, repro or mute) may be selected excluding the other three. Sync monitoring can not be done on a channel being used for recording since it would be impossible to record and play back simultaneously on the same head.

## 3-5 Fast Winding

For fast winding (fast forward or rewind modes), press either REWIND or FAST FWD or the variable speed SHUTTLE. The associated rewind or fast forward indicator lights. For cueing operations, these pushbuttons can be pressed alternately without having to press STOP between fast winding selections, or the variable speed membrane switch can be used. Either fast winding mode can be entered from stop, play, or record mode.

Play mode can be entered while in fast forward or rewind mode by pressing PLAY. Record mode may only be entered from stop or play mode.

The fast forward/rewind variable speed SHUTTLE membrane switch provides variable shuttle speeds. Pressing the switch at the center position results in zero shuttle speed; pressing the switch at its ends results in maximum shuttle speed in the indicated direction. The shuttle speed is made variable between zero and maximum speed by pressing the membrane switch between the center and extreme position of the switch. The control logic latches at the speed selected so that it is not necessary to continue depressing the switch while shuttling. The variable speed shuttle membrane switch is connected in parallel with the FAST FORWARD and REWIND pushbutton switches.

Two tape lifter arms that move the tape away from the heads are actuated in fast winding modes. To monitor audio in these modes (retract lifters), press LIFT

DEFEAT. Since this switch reverses the normal operation of the tape lifters, the tape is lifted away from the heads during play and record modes of operation. LIFT DEFEAT is momentary and is active only while the button is depressed.

#### 3-6 Speed Select

#### 3-7 Fixed Speed Mode

To operate the system at fixed speeds (7.5, 15, or 30 in/s), press the switch corresponding to the desired speed. An LED under the switch lights to indicate operation in the assigned speed.

#### 3-8 Variable Speed Mode

To operate the system at variable speeds proceed as follows:

- STEP 1 Select a fixed tape speed and actuate VSO. (This function is indicated by a flashing yellow LED under the VSO switch.)
- STEP 2 Select units of tones or percent by pressing TONE or %. The tape speed display indicates %6.00 tones (%1 octave) or 50% to 200% of nominal. An LED under TONE or % switch indicates operation of that mode.
- STEP 3 When TONE is selected, pressing DEC decreases speed in 1/4-tone steps on each actuation; pressing INC increases speed in 1/4-tone steps on each actuation. The tape speed continues to increase or decrease if INC or DEC is held depressed.
- STEP 4 When % is selected, pressing DEC decreases the tape speed in approximately 1/10% steps; pressing INC increases the tape speed in approximately 1/10% steps (2/10% in the range of 120% to 200%). The tape speed continues to increase or decrease if INC or DEC is held depressed.
- STEP 5 To cancel VSO operation, actuate any one of the fixed speed membrane switches.

#### 3-9 Monitor Functions

Proceed as follows to activate any monitor function (input, sync, repro, or mute):

- STEP 1 Perform all steps of preoperating procedure.
- STEP 2 Press right- or left-hand membrane switch associated with the monitor function desired (input, sync, repro, and mute). Assign channels to desired function by pressing corresponding channel select switches. The associated indicators (yellow) light.
- STEP 3 If REPRO or SYNC is one of the functions selected, press PLAY to start tape motion and reproduce recorded material. The play indicator (green) lights.

#### 3-10 Recording

Proceed as follows:

- STEP 1 Perform all steps of preoperating procedure.
- STEP 2 Press the right- or left-hand READY. Assign each channel to be recorded by pressing corresponding membrane switch for each channel. The associated ready indicator (yellow) in the LED matrix lights. (When the recorder is initially turned on, all channels previously in record mode are now in ready mode.)
- STEP 3 Assign channels to monitor functions by first pressing the applicable monitor function membrane switch (input, sync, repro, and mute), then pressing the channel membrane switches.
- STEP 4 Connect signals to be recorded to the appropriate audio input connectors.
- STEP 5 Simultaneously press PLAY and RECORD to start tape motion and begin recording on selected channels. (An alternate method is to press PLAY to start tape motion and then, while holding the PLAY pushbutton depressed, press RECORD. Those channel-ready indicators which were vellow will change to red, as will the corresponding VU meters. The RECORD switch indicator will also illuminate.
- STEP 6 While recording, the input signal for each channel can be compared with the recorded signal on that channel by assigning the channel(s) alternately to INPUT and REPRO functions.
- STEP 7 To put additional channels in record, set the channels first to the ready condition, and then press RECORD and PLAY concurrently.
- STEP 8 When recording is complete, record mode may be terminated by performing any one of the following steps. (Note that internal logic control circuitry delays any commanded change in tape motion direction or velocity until after all channels have completely terminated record inode.)
  - a. Press STOP to stop tape motion and deactivate record mode.
  - b. Depress RECORD and momentarily press STOP. Record mode should terminate and transport should continue to run at selected tape speed.
  - c. Press REWIND or FAST FWD.
  - d. Press SAFE or READY and any channel membrane switch. This terminates record for the channel assigned and tape continues to run at the selected tape speed.

#### 3-11 Sel-Sync Function

In Sel-Sync mode (see Figure 3-4), the audio signal to be reproduced from the tape is derived from the record head rather than the reproduce head. This mode of operation permits recording of new material precisely in time with previously recorded material and is used normally for Sel-Sync recording and overdubbing, as described in the following paragraphs.

In Sel-Sync recording, a performer listens to one or more previously recorded tape tracks while recording material on another track. For example, assume a 24-channel recorder is equipped with a tape having 12 prerecorded tracks and 12 blank tracks. Typically, the 12 prerecorded tracks are reproduced (using the record head for pickup), mixed together using studio equipment, and fed to a performer's headphones. The performer then listens to the prerecorded material while recording material on one of the blank-track channels. Thus, the new material is recorded synchronously with the prerecorded material.

In overdubbing, a performer listens to material that he previously recorded on one or more tape tracks. At the same time the performer repeats his previous performance to get into proper timing with the original material without actually recording. At the point where the overdub is desired, the tracks to be overdubbed are switched to the record mode. The audio that the performer hears in the process is automatically switched from the off-tape audio to the input audio the performer is recording; that is, from sync monitoring to input monitoring. Alternatively, switching may be made from sync to repro or mute monitoring if programmed by the monitor memory R mode (see monitor memory programming in paragraph 3-13).

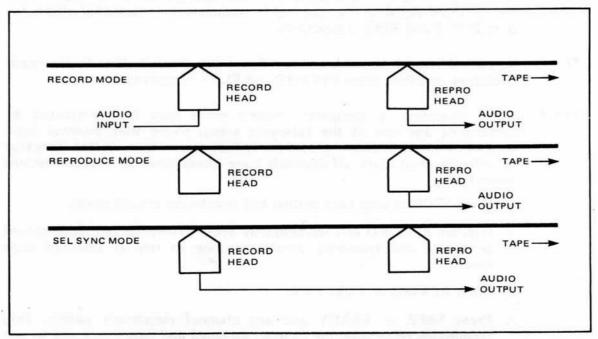


Figure 3-4. Head Usage for Different Operating Modes

To place a channel in Sel-Sync mode, proceed as follows:

- STEP 1 Perform all steps in preoperating procedure.
- STEP 2 Press SYNC. Assign the desired channels for the Sel-Sync mode by pressing the membrane switch corresponding to the channel. Any channel which is now placed in ready will automatically switch to input mode when record mode is activated.
- STEP 3 Follow instructions for recording or reproducing depending on desired Sel-Sync mode of operation.

#### 3-12 Groups

The group switching feature allows any number of channels to be attached to a group so that group can be controlled by a single switch. There are four groups numbered G1 through G4, and each has functions and indicators identical to those of the individual channel. To attach channels to a group:

- STEP 1 Press the right- or left-hand GROUP switch.
- STEP 2 Press a group number switch (G1-G4). The selected switch LED lights.
- STEP 3 Select and push switches of the individual channels to be entered into that group. Individual channel LEDs light when attached to a group. Alternatively, all channels may be attached to a group through the ALL switch.
- STEP 4 Enter group into a particular monitor and/or ready/safe status by pressing the associated function switch and group number (G1-G4) switch.

To determine which channels have been attached to groups, the groups must be interrogated one at a time. This is done by pressing GROUP, then a group number switch and observing which channel indicators light up.

A channel remains attached to a group until it is intentionally detached. To detach a channel from a group:

- Attach it to a different group.
- Clear it from a group by pressing GROUP, GC, and individual channel-select switch.
- Clear all channels from a group by pressing GROUP, GC and group number (G1-G4).
- Clear all channels from all groups by pressing GROUP, GC, and ALL.
- Select a function for that individual channel different from the function selected for the group.

#### 3-13 Monitor Memory

The monitor memory can be used to preprogram the monitor functions (input, sync, repro, mute) so that they are automatically selected with changes in transport mode (record, play, fastwind, stop). Thus, individual channels may be programmed for different monitoring functions under the same transport mode and programmed for a different monitoring function arrangement under another transport mode. The monitor memory includes five MONITOR MEMORY switches: R (record), P (play), F (fastwind), S (stop), and TRANSFER.

The monitor memory array can be programmed for the current transport mode of operation, or it can be set up for a mode other than the current transport mode of operation. To activate the monitor memory for a transport mode of operation either for the one in use or for any other mode, press the desired pushbutton (R, P, F, or S). Then, with the associated pushbutton LED on, assign the channels to monitor functions (input, sync, repro, or mute). The selection is stored in the monitor memory. When a transport mode is entered, channels will be monitored as preselected for that mode. (Note: R, P, F, or S flash if selected for a mode different from the current transport mode. The actual monitoring stays with the current transport mode, not the panel display.)

The TRANSFER switch is used to duplicate one (or more than one) monitor setup into another transport mode. In this way, a new array need not be set up for each transport mode. The monitoring array programmed for one mode may be entered unaltered into any other transport mode's monitor memory by using the TRANSFER switch. To transfer an array from the selected transport mode to another mode, press TRANSFER (the switch will flash) then press the desired transport mode switch on the monitor memory.

The monitor memory function is normally inactive and must be activated each time it is used. The inactive condition is indicated by the R, P, F, S indicator LEDs all being off. To deactivate the monitor memory without turning power off, select the stop transport mode and press the illuminated MONITOR MEMORY S (stop) switch. The switch LED goes out, and the monitoring functions left in the memory associated with the S (stop) switch apply to all transport modes.

Because it is inconsistent to have sync monitoring at the same time that the recorder is in record or rehearse, those channels entering record or rehearse will change from sync to input monitoring. When the record or rehearse mode is terminated, the input monitoring will change back to sync monitoring.

## 3-14 Multiple Setup Memories

The setup memory is used to store up to four complete signal switching setups. Each setup includes the recording functions, monitoring functions, group functions, and monitor memory for all channels. One setup memory at a time is selected to exercise control over the signal system. The setup memories are selected by four setup memory switches labeled A, B, C, and D. A yellow LED is lit under the switch for the memory selected. A different setup is selected by

actuating an unlighted switch. The contents of the displayed setup memory can be duplicated in another memory by first actuating the TRANSFER switch and then actuating the desired memory switch. The receiving memory is automatically selected by this action as the LED indicators show. The yellow LED under the TRANSFER switch is on and flashing from the time the TRANSFER switch is actuated until a memory switch is actuated.

If the operator decides not to transfer anything after the TRANSFER switch is actuated, this function can be canceled by actuating STOP or any other transport mode switch. The transfer function can also be canceled by selecting any signal switching function other than a setup memory, or by pressing the memory switch which was already lit.

The ability to change the setup memory selection is inhibited while any channel is in the record mode.

#### 3-15 PURC Operation and Editing

The recorder is capable of operating with or without PURC, as desired.

The use of PURC eliminates the problem of overlaps and holes in recordings when inserting (dubbing) new material within previously recorded programs. In a recorder system without PURC, initiating record mode energizes the erase and record heads simultaneously. Since there is a physical distance between the erase and record heads, a period of over-recording on unerased tape occurs. When the dub is terminated, a hole is left in the program. The length of time of this hole is related to the distance between the erase and record heads and the speed of the tape.

In a system equipped with PURC, separate erase and bias amplifier circuits are provided, and the turn-on and turn-off times of the amplifiers are individually controlled. When the record mode is initiated, the erase circuit is energized first; then, after a time interval, the bias amplifier is energized. When the recording is terminated, the erase circuit is deenergized first; and then, after a time interval, the bias amplifier is deenergized. Thus, the problem of an overlap and a hole is eliminated in the dubbed portion of the recording. These on and off times are illustrated in Figure 3-5.

The approximate on- and off-time delay to be considered while performing PURC edit functions is calculated by dividing the distance between the erase and record head by the tape speed. These approximate on/off delay times are shown in Table 3-5.

## 3-16 Tape Timer Operation

The tape timer displays in hours, minutes, and seconds the distance the tape has moved from a zero reference (0:00:00) point established by pressing TIMER RESET on the control panel. The timer displays +0:00:00 to +9:59:59 when the transport operates in the forward direction, and displays -0:00:00 to -9:59:59 after passing through +0:00:00 when operating in the reverse direction. If the tape runs off either reel, the tape timer display freezes.

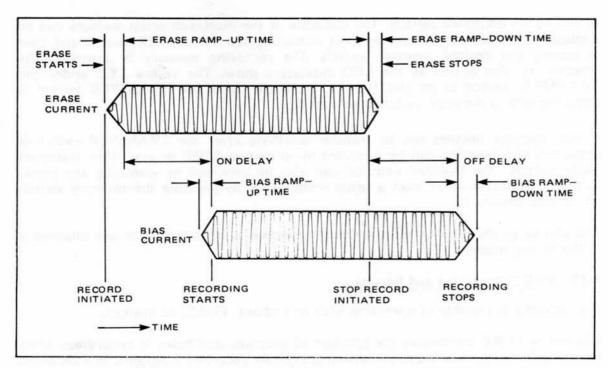


Figure 3-5. PURC On/Off Timing Relationships

Table 3-5. PURC On/Off Timing Relationships

Tape Speed	Approximate On/Off Delay Time
30 in/s	75 ms
15 in/s	150 ms
7.5 in/s	300 ms

Pressing the TIMER RESET pushbutton switch on the remote control unit or on the recorder/reproducer control panel resets both tape timer displays to 0:00:00.

#### 3-17 Remote Control Operation

All recorder functions can be controlled from the remote control unit except servo disarm. The remote control unit operates in parallel with the local unit at all times and is self-powered.

#### 3-18 Single-Point Search-To-Cue (SPSTC)

#### Note

The multipoint search-to-cue (MPSTC) is an optional accessory. See manual No. 4890426 for operation and service instructions.

Pressing SEARCH causes the tape to be shuttled at fast speed to a cue point previously selected by pressing CUE STORE. A search can be initiated from any

transport mode as long as the reel servos are armed. Actuating SEARCH terminates the previous mode and leaves the transport in the stop mode at the end of the search. The play mode is entered automatically at the end of the search if PLAY is actuated anytime after SEARCH is pressed and before the search ends. If the play mode is to follow the search mode, the upper PLAY indicator lights until the search is finished and the lower PLAY indicator lights when play speed is obtained and stabilized.

Perform the search function as follows:

- STEP 1 After threading tape on the transport and activating reel servos, set tape timer to 0:00:00 by pressing TIMER RESET. A point other than beginning of tape may be selected as tape timer 0:00:00, if desired, by pressing TIMER RESET at that point.
- STEP 2 When a desired cue point is reached, press CUE STORE. The search-tocue circuit stores this position (not tape time) in a memory. Cue point counter is independent of tape timer counter. Tape timer reset, therefore, does not disturb cue point location.
- STEP 3 To search to the preselected cue point, press SEARCH.
- STEP 4 To select a different cue point, press CUE STORE when new cue point is reached.

#### 3-19 Single Point Search-To-Cue (SPSTC) Looping

During single point search-to-cue looping, a given length of tape is automatically replayed repeatedly.

Proceed as follows to replay a designated length of tape:

- STEP 1 Press CUE STORE at beginning of designated tape length.
- STEP 2 Shuttle tape to end of designated tape length; then while pressing SEARCH/CUE, press TIMER RESET.
- STEP 3 Press STOP to terminate looping.

#### 3-20 Record Lockout

There are three ways to prevent a channel from going into record mode even though set for the ready condition on the setup panel:

 Press RECORD INHIBIT on the secondary control panel. This opens all Audio PWA relays in series with the erase and record heads and inhibits the microprocessor from selecting record for any channel. The rehearse mode may be selected, however.

#### Note

Do not press the RECORD INHIBIT switch while in record. If any channel is in record and the switch is pressed, the relays will open but the electronics will stay in record. If the switch is pressed again, the relays will close, returning the channel to normal record.

- Install record lockout jumper J3 (Figure 3-6) on Main CPU PWA in A-B position. This jumper is in parallel with RECORD INHIBIT switch on the secondary control panel and provides a more positive lockout since the operator has less access to this jumper than the switch. The B-C position of the jumper is the normal position.
- Install record inhibit jumper J201 on an individual Audio PWA in the B-C position. This prevents the channel from going into record or rehearse even though the setup panel indicates record for the channel. Also, the associated VU meter will not illuminate in red. Jumper position A-B is normal for record. Jumper J1 is useful in protecting a time-code track from being erased accidently.

#### 3-21 End-of-Tape Stopping

The capstan servo/transport control PWA switch S1-1 (Figure 3-7) provides the alternative of either letting the tape stop before it unwinds completely or letting the tape wind off completely at play speed. Set S1-1 up for tape stop or down for play-off.

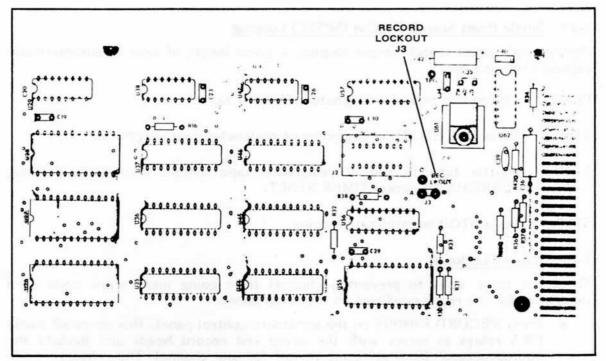


Figure 3-6. Main CPU PWA - Record Lockout Jumper J3-Location

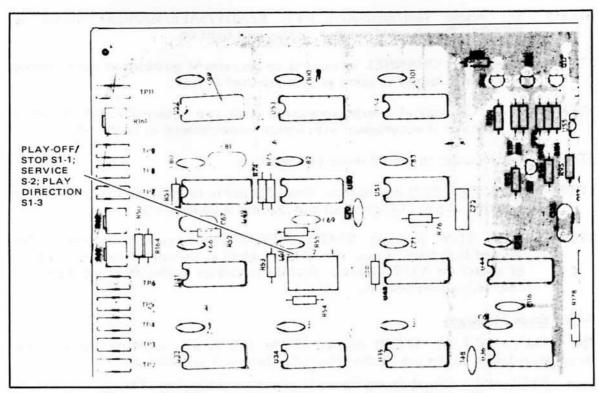


Figure 3-7. Capstan Servo/Transport Control PWA—Play Off/Stop Switch S1—Location

#### 3-22 Manual Wakeup

If a problem should arise during machine operation, such as receiving an improper response during program sequencing, the problem may be resolved by restarting program operation. This is accomplished by pressing the MANUAL WAKEUP switch on the Capstan Servo/Transport Control PWA (Figure 3-7) without destroying the RAM contents.

#### 3-23 Auto-Bias Operation

Auto-bias operation is associated with the Audio Test/Auto-Bias PWA accessory described in paragraph 1-13. Auto-biasing is an alternative to the manual biasing level adjustments set through the master bias potentiometers on the VSO PWA and described in paragraph 5-39 of Section 5. Auto-biasing overrides manual adjusted biasing when the READY/SAFE/MANUAL switch of the Audio Test/Auto-Bias PWA is set to READY or SAFE. Manually adjusted biasing is in control when the switch is set to MANUAL or the Audio Test/Auto-Bias PWA is removed from the recorder.

Once the auto-bias level has been set, it will hold that level indefinitely in a digital memory backed up by the battery supply. When a new bias level is required it can be set as follows:

STEP 1 Choose blank track for a test track and set that channel into READY and REPRO on the recorder setup panel.

- STEP 2 Set Audio Test/Auto-Bias PWA READY/SAFE/MANUAL switch to READY. The channel number display will light up.
- STEP 3 Press PWA CHANNEL increment or decrement pushbutton until number on channel display is same as that selected in step 1.
- STEP 4 Select amount of overbias required with two rotary OVERBIAS select switches or in accordance with levels recommended in Table 5-9.
- STEP 5 Set recorder in record mode of operation.
- STEP 6 Press PWA RUN pushbutton. Red LED lights to indicate calibration is in progress. When LED goes out the process is completed.
- STEP 7 Press STOP and set READY/SAFE/MANUAL switch to SAFE. The desired bias level is now stored and locked in memory. Note that setting of switch to SAFE position disables auto-bias calibration and turns off channel number display.

#### 3-24 Error Messages

The setup panel TAPE SPEED display (Table 3-2) is also used to display error messages relating to the use of the recorder. These are as follows:

- ERR1 ISL illegal speed. Speed selected on setup panel VSO section has its
  equalization turned off on secondary control panel.
- ERR2 LKD servos locked. A play or record command was given and transport did not lock on speed within 3 seconds in record or 15 seconds in play.
- ERR3 MTS motion sense. A stop command was given and tape did not stop moving within 7 seconds. (Displayed only when the monitor memory, R, P, F, or S, is active.)
- ERR4 ERS electronic record status stuck high. A record command was given but recorder did not enter record within 2 seconds. Monitoring reverts to play mode.
- ERR5 ERS electronic record status stuck low. Record stop command given but recorder did not exit record within 2 seconds.

# SECTION 4 THEORY OF OPERATION

#### 4-1 INTRODUCTION

This section of the manual provides a block-diagram-oriented discussion of the ATR-116/124 recorder/reproducer system followed by detailed theory of operation. Figure 4-1 is a simplified block diagram of the ATR-116/124.

#### 4-2 FUNCTIONAL DESCRIPTION OF THE TAPE TRANSPORT

The recorder/reproducer controls tape movement in all modes of operation while under capstan servo and reel servo control. The capstan servo controls tape speed and direction while a reel servo maintains dynamically constant tape tension in all modes of operation. The capstan is driven to control tape motion without the use of a pinch roller. The actual work of moving the tape, however, is accomplished by the reel servo which operates independently of the capstan servo. Near-equal tape tension is maintained on the takeup and supply side of the capstan for all sizes of tape reels. Since there is little difference in tape tension at the capstan, there is no tendency for tape to slip on the capstan and therefore no pressure roller (pinch roller) is required.

Tape tension in the reel servo loop is controlled by dc reel motors and tension arm springs which are a component of tape tension arm assemblies. The tension arm springs apply a force to the tension arms that is opposed by the force provided by the reel motors through the tape. The tension arms have a differential transformer sensor affixed to each arm. The output from the sensor is a voltage indicative of arm position and is the servo error.

Tape motion creates an imbalance or position error of the tension arm's position and, by means of the reel servo, a tension imbalance is created in the tape path (but not across the capstan) by the reel motors. This tension imbalance causes the reel motors to perform the work of moving the tape at a rate established by the capstan. There are no independent commands supplied to the reel servo to cause such an imbalance. All control of the reels is initiated by capstan movement transmitted through the tape to the tension arm sensors and by a direction sense from the capstan servo.

The output from the tension arm sensors is amplified, compensated for the mechanical properties of the transport, and used to modulate a 28.8 kHz carrier to develop a pulse-width modulated (PWM) signal with a duty cycle that varies according to the magnitude of the servo error signal. The PWM signal is amplified and used to drive the dc reel motors.

#### 4-3 GENERAL OPERATIONAL DESCRIPTION

The ATR-116/124 performs record/reproduce operations on up to 16/24 channels under several operational modes. The following paragraphs elaborate on this.

#### 4-4 Servo-Limited and Full Torque Condition

After operation is initiated and tape is pulled taut, the reel servos are activated and assume a limited torque condition. After the servo-limited torque condition is established, any operating mode can be entered. Upon entering that mode, a full torque range is established.

#### 4-5 Reproduce (Play) Mode

When play mode (or record mode) is selected, the capstan motor is initially driven by a fixed dc current source until a phase-lock condition is achieved. The motor is then controlled by the output of a phase comparator on the Capstan Servo PWA. The inputs to the phase comparator are a submultiple of a 9600-Hz reference frequency and the capstan tachometer pulses from the capstan assembly. The submultiple frequency used is dependent on the tape speed. As already discussed, tape movement is sensed by sensors on the tension arms, which direct the reel servos to cause tape reel movement. The audio signal recovered from the tape by the reproduce head or record head (Sel-Sync operation) is preamplified on the Audio-Preamp PWA and then amplified and equalized on the Audio PWA. This signal is then routed to audio output connectors for external use.

#### 4-6 Record Mode

In the record mode, tape is moved across the heads under reel servo and capstan servo control, as in play mode. Erase (144-kHz) and bias (324-kHz) signals from the Variable Speed Oscillator (VSO) PWA are available at all times at the respective erase and bias input of each channel Audio PWA, via erase and bias buses. In the record mode for a particular channel, the erase signal applied to the channel Audio PWA is amplified and fed to the erase head to erase any previously recorded signals from the tape before it reaches the record head. Information to be recorded is applied to the Audio PWA where it is combined with the bias signal, amplified, and applied to the record head. The information is recorded on the tape as it passes over the record head. However, actual recording on tape is not permitted to begin until a phase-locked signal from the Capstan Servo/Transport Control PWA is received by the Main CPU PWA. During recording, bias and erase status signals are routed through meter lamp logic on the Audio PWA to the red meter lamp. Lamp operation (continuous red) indicates all prerequisites to record mode are present.

#### 4-7 Shuttle Modes

When the machine control panel FAST FWD or REWIND switch, or the setup panel, SHUTTLE touch bar is activated, the capstan is driven by a dc voltage driver rather than the phase comparator circuit. As in play and record modes, the tape movement is sensed by the supply and takeup sensors on the tension arms and, by means of the closed-loop reel servo, tape is moved from reel to reel,

#### 4-10 System Wakeup Circuit

Transistors Q1 and Q2 (Figure 4-2 and Schematic No. 4840473) and associated components comprise a system wakeup circuit that causes the recorder to be in the stop and servo-off modes as power is turned on. This circuit also causes the SPSTC tape timer to be reset to indicate 0:00:00.

When power is first applied, capacitor C32 charges through resistor R13, causing transistor Q2 to turn on during the charging interval. With Q2 on, transistor Q1 turns on providing logic low wakeup command. After approximately 6 seconds, C32 is charged and causes Q1 and Q2 to turn off, and the wakeup line goes high. The 6s delay is applied to other delay circuits on other units of the recorder (Figure 4-3) where they are used to generate master reset signals. In the event power is lost and reapplied before the cycle is completed, CR2 quickly discharges C32 to permit a complete wakeup cycle when power is reapplied.

A manual wakeup feature is provided through switch S4 which parallels the transistor Q1/Q2 arrangement. When S4 is pressed, the wakeup line goes low, as during power up, to activate the signal. Its use is employed if the microprocessor should become erratic during software operations, as evidenced by erratic machine behavior. When S4 is activated, a program sequence is restarted without causing erasure of the RAMs.

#### 4-11 Transport Control Functional Description

The transport control portion of the Capstan Servo/Transport Control PWA (Figure 4-2 and Schematic No. 4840473) accepts input commands from the machine control panel (or machine remote control panel) and status signals from other circuits within the recorder system, and performs logic functions that are used to control all transport functions and modes of operation.

## 4-12 Control Circuit Operation

A mode of transport operation is selected by pressing a pushbutton switch on the machine control panel. This generates a logic low that sets an associated latch. The latches are interconnected to make the operation mutually exclusive. Therefore, only one mode may be engaged at a time. The output of the latch also causes the associated indicator to light through the turn-on of a transistor switch.

## 4-13 Tape Lifter Operation

The tape lifters lift the tape away from the heads when FAST FWD, REWIND, or SHUTTLE is pressed. The shuttle command, which is generated when shuttle latch U30-8, U31-12 is set (paragraph 4-26), sets tape lifter latch U24-6, U24-8. The resulting high from U24-6 is inverted and routed to exclusive OR-gate U6-6. In normal operation a high lift command is then routed from U6-6 to the tape lifter solenoid and the tape is lifted from the heads.

If the play mode is selected while operating in the fast forward mode, play latch U30-6, U30-12 is set, which causes shuttle latch U30-8, U31-12 to reset; the tape subsequently slows down to the play speed selected. Upon reaching play speed, tape lifter latch U24-6, U24-8 is reset by the servo locked command. This causes the tape-lifter solenoid to be deenergized and the tape lifter to retract.

If the stop mode is selected from any mode, the play or shuttle latch, as the case may be, is reset. If the tape is permitted to stop, the tape lifter latch is reset by the motion sense command from long time constant one-shot U17-10 as it times out.

Tape lifter operation is defeated by pressing LIFT DEFEAT. Pressing the push-button routes a logic low lift defeat (LDB) signal to exclusive OR-gate U6-6. If the machine is in play or stop mode, the lifter latch U24-6, U24-8 is not set, and the logic low LDB signal is inverted by U6 to a high and routed to the lifter solenoid. The lifter solenoid then lifts the tape from the heads. If, however, the machine is in fast forward or rewind mode, the lifter latch is set and the logic low LDB signal causes the output of exclusive OR-gate U6 to change from a high to a low. This low signal deenergizes the lifter solenoid, and the tape returns to the heads.

#### 4-14 Play Mode

Pressing PLAY causes play latch U30-6, U30-12 to set. The play command output low is routed from gate U16-8 to the capstan servo circuit and to circuitry on the Main CPU and VSO PWAs.

#### 4-15 Record Mode

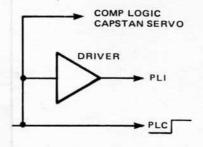
The record mode is selected by simultaneously pressing PLAY and RECORD. Pressing PLAY generates a signal that resets stop latch U31-6, U31-8. Upon entering record mode, a low electronic record status (ERS) is received by the PWA from the Audio Control PWA. This low activates the electronic record status indicator (ERSI) signal which results in the lower half of the record indicator being illuminated, thus signifying that record mode has been established. If STOP is pressed while in record, the transport motion does not stop until the bias and erase signals applied to the record and erase heads, respectively, have decayed (ERS command goes high).

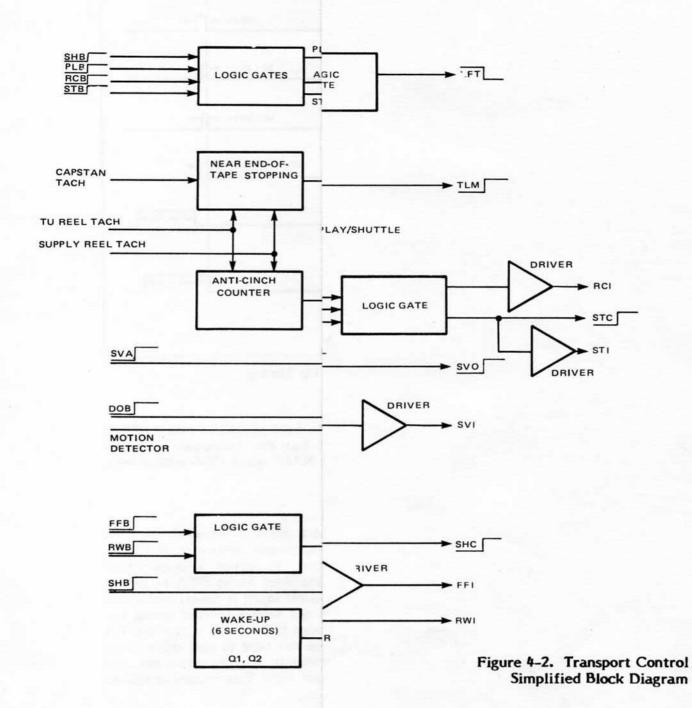
ERS occus when any channel goes into Record (Bins ranged on).

See Audio Control Board operation - pg. 4-51.

Upper lamp of REC bettern is untolled by STC board in Control Ray (schematic missing)...

Capstan Servo Bd.





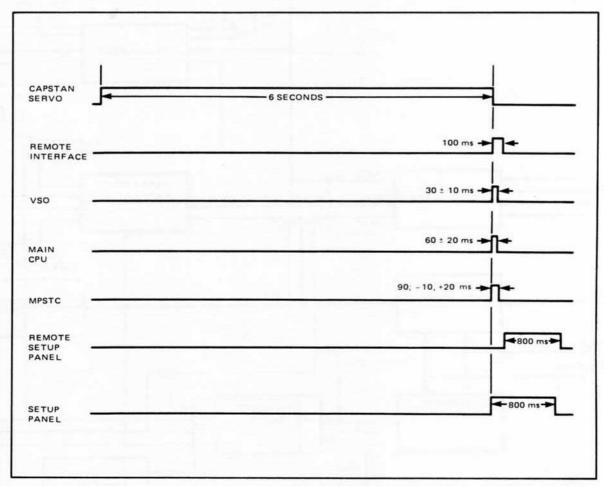


Figure 4-3. ATR-116/124 Wake-Up Timing

#### 4-16 Stop Record Mode

If the recorder is in record mode and RECORD is held pressed while STOP is momentarily pressed, the recorder stops recording but the transport continues running. Tape motion stop is prevented by inhibiting NAND-gate U7-6 with a logic low that is generated when RECORD is pressed.

#### 4-17 Limited Torque and Anti-Cinch Circuit

When tape is first threaded and before any transport mode is entered, the reel servos are in a torque limited mode (TLM). That is, torque limit circuit U27-3, U27-6 is latched and sends a low TLM command to the reel servos. This command switches the reel servo compensation amplifier on the Reel Servo PWA to torque limit. When a transport mode is entered, the torque limit latch is reset, and a full torque range is then available to the reel servos. In the torque limited mode, the reels can be threaded so that they hold tape tight enough to keep the servos on, but the tape may not be secure to the hub. This can cause the tape to jerk the tension arms, generating a very large tension error. To compensate for this error, the reel servo causes the reel motor to feed tape at a very fast rate. This results in spilled

tape and possible tape damage. The anti-cinch circuit prevents this condition from happening. Entering any mode cancels the anti-cinch feature.

Anti-cinch circuit U52, U54 counts reel tach pulses. If the number of pulses generated before a mode is entered exceeds 15 (about 1/3 to 1/2 reel revolution), the anti-cinch latch U35-11, U43-6 is set. Setting the latch generates a shutdown pulse and the servos are shut down. To thread tape, the torque limit condition (tape taut against tension arms) must be re-entered. When the transport enters any mode, the resetting of torque limit latch U27-3, U27-6 disables anti-cinch circuit U52, U54.

#### 4-18 Servo Disarm Button

Pressing the REEL SERVO DISARM pushbutton on the machine panel generates a low servo disarm command (SDB). (There is a REEL SERVO DISARM indicator on the remote control panel, but it serves as an indicator only.) The SDB command is routed to the Capstan Servo/Transport Control PWA where it sets servo disarm latch U35-3, U28-12. The output of the latch is used to generate a logic high SVO signal. This signal is routed to the reel servo PWAs, shutting the reel servos off. The signal is also routed to transistor Q10. Q10 then turns on, which in turn provides a ground to light the REEL SERVO DISARM indicator. The servo disarm latch is also set by the wakeup line during power application. Capstan servo operation can be maintained regardless of transport mode (even if tape is not threaded) by setting service switch S1-2 (Figure 3-7) on the Capstan Servo PWA to the service position.

#### 4-19 Capstan Servo Functional Description

The capstan servo controls the speed and direction of the dc capstan motor during all recorder modes of operation. Figure 4-4 is a block diagram of the capstan servo system. During operation, tachometer pulses are generated at a rate proportional to speed. These pulses are amplified, shaped, and fed as one input to a digital phase comparator. The other input to the phase comparator is a reference signal, whose frequency is made dependent on the tape speed selected. This reference signal is derived from a master oscillator and determines the speed of the machine. During play operation, when the phase comparator is locked to the two signals, a phase-modulated rectangular wave error signal is provided by the phase comparator. This signal is fed through a carrier filter and a compensation amplifier, which compensates for the mechanics of the system, to the capstan motor drive amplifier (MDA). The MDA drives the dc capstan motor.

During the initiation of stop mode, and during the initiation of play or record modes before phase lock is achieved, the capstan motor is controlled by a fixed do current source from an acceleration driver. The direction of current through the motor causes its acceleration in the play/forward modes and deceleration in the stop mode.

#### 4-20 Capstan Servo Circuit Details

The capstan servo circuitry is principally located on Capstan Servo Transport Control PWA, in the tach preamp and in the power supply assembly. Figure 4-5 is a simplified block diagram of the capstan servo. See also Schematics 4840473, 4840481, and 4840499).

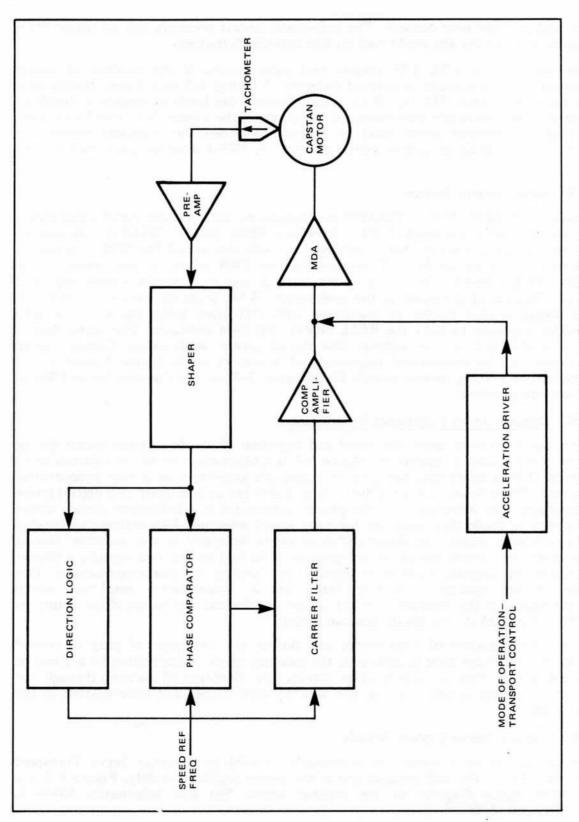
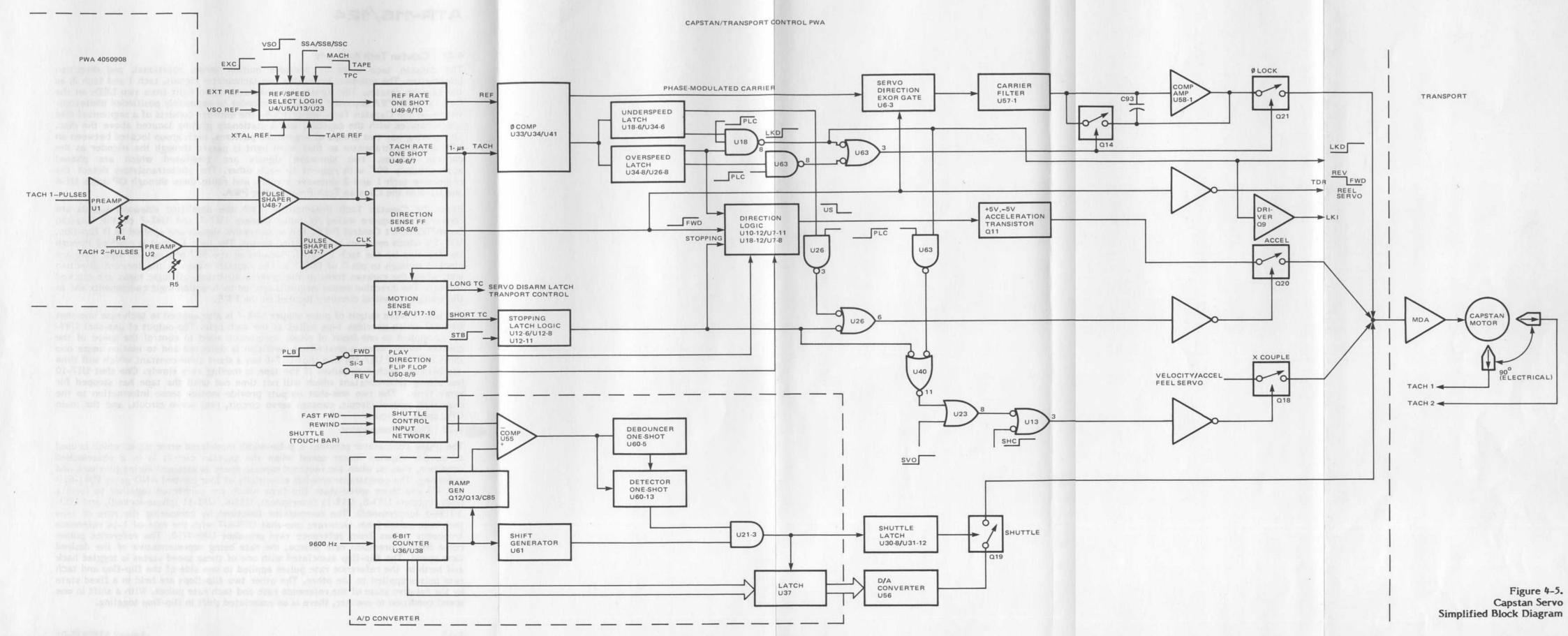


Figure 4-4. Capstan Servo-General Block Diagram



#### 4-21 Capstan Tach Assembly

The capstan tach assembly provides motion sense, rotational, and direction information. The assembly generates two tachometer signals, tach 1 and tach 2, as the capstan rotates. The signals are generated when light from two LEDs on the Capstan LED PWA is passed through an encoder to oppositely positioned phototransistors on the Capstan Tach Sensor PWA. The encoder consists of a segmented disc which rotates with the capstan, and a stationary grating located above the disc. The grating has two groups of segmented patterns, each group located between an LED and phototransistor so that when light is passed through the encoder as the capstan rotates, two sinewave signals are generated which are phased approximately 90° with respect to each other. The phototransistors detect the respective tach 1 and 2 sinewave signals, and route them through OP amps U1-6 and U2-6 on the Capstan Tach Preamplifier PWA.

From the Capstan Tach Preamplifier PWA the amplified sinewave signals are converted to square waves by pulse shapers U47-7 and U48-7 of the Capstan Servo/Transport Control PWA. The square-wave signals are applied to D flip-flop, U50-5/6 which operates as a direction sensor. The tach 1 signal is clocked through the flip-flop by the tach 2 signal. Because of the 90° phasing, all logic lows are clocked through to pin 5 of U50-5 as the capstan moves in the forward direction and, when the capstan turns in the reverse direction, all logic highs are clocked through. The direction sensor output is applied to direction logic components and to the transport control circuitry located on the PWA.

The square wave output of pulse shaper U48-7 is also applied to tach rate one-shot U49-6/7 which provides 1-µs pulses at the tach rate. The output of one-shot U49-6/7 is applied to one input of phase comparator used to control the speed of the capstan motor when a phase-lock condition is detected and to motion sense one shots U17-6 and U17-10. One shot U17-6 has a short time-constant which will time out between tach rate pulses if the tape is moving very slowly. One shot U17-10 has a long time-constant which will not time out until the tape has stopped for some time. The two one-shot outputs provide motion sense information to the transport control circuit, capstan servo circuit, reel servo circuit, and the main CPU control circuit.

#### 4-22 Phase Comparator

The phase comparator provides a pulse-width modulated error signal which is used to control capstan motor speed when the capstan circuit is in a phaselocked condition, that is, when the required capstan speed is attained during playback and recording. The comparator consists essentially of four control AND gates (U41-6, 8 and 11) and three speed-state flip-flops which are connected together to form a shift register: U33-8, U33-11 (overspeed), U33-6, U33-11 (phase-locked), and U33-3/U34-3 (underspeed). The comparator functions by comparing the rate of 1-µs tach-rate pulses from tach-rate one-shot U49-6/7 with the rate of 1-µs reference frequency pulses from reference rate one-shot U49-9/10. The reference pulses come from a precision rate source, the rate being representative of the desired tape speed. The flip-flop associated with one of these speed states is toggled back and forth by the reference rate pulses applied to one side of the flip-flop and tach rate pulses applied to the other. The other two flip-flops are held in a fixed state by the relative state of the reference rate and tach rate pulses. With a shift in one speed condition to another, there is an associated shift in flip-flop toggling.

Reference frequency pulses which are applied to reference rate one-shot U49-9/10 are derived from a 9600-Hz crystal oscillator located on the VSO PWA (which is independent of VSO circuitry) from a variable frequency (VSR) source from the VSO circuitry, or from some tape reference or other external source which is received through the I/O panel accessory connector. The reference frequency is passed to an input of an OR-gate (U23-3, 6, or 11). The other input to the particular U23 gate receives an enabling logic low signal to pass the reference signal through the gate to a coincidence reference detector circuit. The detector circuit is not used and not essential for processing the reference signal. Its function is to provide a smooth transition in the change-over from one source to another when employed. The enabling logic low is present to pass the 9600 Hz reference frequency from the VSO PWA through OR-gate U23-11 if external reference or VSO reference (VSR) signals are not selected. If one of these latter two is selected, an enabling logic low must be generated from one of the two sources to enable the respective U23-3 or U23-6 gate.

The reference signal output from the detector circuit is applied to frequency divider U4, which outputs the divided frequencies to speed selector U5. Speed Selector U5 is under control of speed select logic from the Main CPU PWA; SSA (pin 89), SSB (Pin 88), and SSC (pin 87). For 7 1/2 in/s tape speed and a 9600-Hz source reference frequency, a 1200-Hz rate is selected and routed through U5 to 1-µs reference rate one-shot U49-9/10. Similarly, for tape speeds of 15 and 30 in/s, divided down reference rate signals of 2400 Hz and 4800 Hz are respectively selected and routed to the one-shot. The 1-µs outputs from one-shot U49-9/10 are routed to phase comparator U33/U34/U41. Table 4-2 summarizes the tape speed-reference frequency relationships which are employed.

Initially, as the capstan speeds up from a stop position to the required playback or record speed, the rate of reference pulses from reference rate one-shot U49-9/10 to the comparator exceed the rate of tach pulses from tach rate one-shot U49-6/7 to the comparator (Figure 4-6). The recorder is then in an underspeed condition, and underspeed flip-flop U33-3, U34-3 is toggled into one state by a tach pulse as the tach pulse is generated and then to the other state by a succeeding reference pulse. This phasing condition of tach and reference pulses also keeps the phase-locked and overspeed flip-flops each in a non-toggling state.

Table 4-2. Tape Speed Reference Frequencies

Tape Speed (In/s)	Mode	Reference Frequency
30	Play/Record	4,800 Hz
15	Play/Record	2,400 Hz
7.5	Play/Record	1,200 Hz
VSO	Play/Record	Variable
Ext Ref	Play/Record	Variable from external source
Tape Ref	Play/Record	Variable from external source

As the capstan motor increases in speed, the frequency of the tach pulses will also increase. A point will be reached where the tach rate will momentarily exceed the reference rate (Figure 4-6). This will cause two tach pulses to appear between two successive reference pulses. The first tach pulse will change the state of underspeed flip-flop U33-3/U34-3 and cause the pin 13 enabling input of AND gate U41-11 to go high. The second tach pulse will be routed through U41-11 to change the state of sync-locked flip-flop U33-6, U33-11, causing U33-6, U33-11 to toggle with each succeeding and alternate tach and reference pulse. At the same time underspeed flip-flop U33-3, U34-3 will be held in a fixed state by the tach and reference pulse phasing. The output of the comparator from U33-6 (TP2) of the phase-locked flip-flop is a pulse width modulated representation of the phase error of the capstan. This output is applied to carrier filter U57-1 which removes the carrier. The signal level at the filter output is a true dc representation of the phase error of the capstan, applied through compensation amplifier U58-1, which compensates for the mechanics of the system. Integrating capacitor C93 in the feedback path of US8-1 provides the capstan servo with a great amount of steady state siffness in the phase-locked condition. The output of the compensation amplifier is applied through phase-lock switch Q21, also under control of the comparator, to the inverting input of op-amp U58-7 of the MDA which is a current mode (high output impedance) amplifier when the recorder is not in the fast forward, reverse, or other shuttle operation. The other non-inverting input to U58-7 receives current feedback through a sensing resistor in the capstan motor armature circuit for stabilizing motor operation.

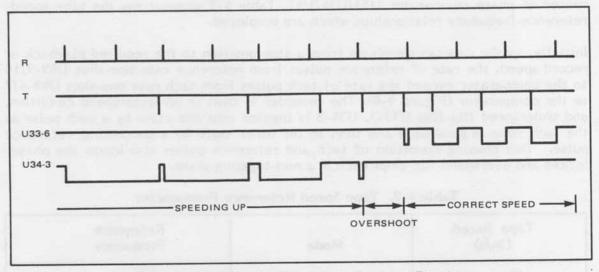


Figure 4-6. Capstan Phase Comparator Phasing

When phase lock flip-flop U33-6, U33-11 toggles to provide the pulse-width modulated error signal as described above, the first positive high appearing at U33-6 of the flip-flop is inverted by gate U26-11 and applied as a reset pulse to latches U34-8, U26-8, U34-6. The first of these latches is set by underspeed flip-flop U33-3, U34-3 to disable phase-locked AND gate U18-8 when the system is in the underspeed condition. The second is set by the overspeed flip-flop to disable U18-8 when the system is in an overspeed condition. The reset pulse applied to

these latches when the phase-lock flip-flop toggles, provides two enabling inputs to phase-lock AND gate U18-8. A third enabling input comes about with the activation of the play command (PLC) signal. The resulting phase-locked logic (LKD) from U18-8 is applied to shunt switch Q14 in the feedback path of the compensation amplifier, turning Q14 off and thereby inserting steady state stiffness integrating capacitor C93 in the feedback path. The logic is also applied to phase-lock switch Q21, turning it on to permit the output of the compensation amplifier to be applied to the MDA in the play and record operating modes.

During the overspeed state, phase-lock control conditions on the capstan PWA exist despite the fact that phase-locked AND gate U18-8 is disabled as described above. In the overspeed state, overspeed latch U34-8/U26-8 is set to provide an enabling high to a bypass AND gate, U63-8, causing shunt switch Q14 to turn off and phase-lock switch Q21 to turn on as in normal phase-lock play conditions. Negative drive is thereby provided to the capstan motor to slow it down. The phase-locked, LKI, logic level signal to the Main CPU and STC PWAs, however, is not generated in the overspeed condition.

Shunt switch Q14 is turned on during the underspeed condition, thereby shorting out C93. This prevents motor overshoot when the motor is coming up to speed in the play/record modes.

#### 4-23 Capstan Direction/Speed Control Logic

The capstan direction/speed control logic provides direction and speed control of the capstan motor in modes other than fast forward, rewind, and variable speed shuttle. It was indicated earlier that in normal operation a pulse width modulated error signal from phase-locked flip-flop U33-6/U33-11 of the phase comparator is used to provide speed control to the capstan motor. Prior to phase lock, however, acceleration transistor Q11 is used to provide drive to the capstan motor to bring it up to speed. Q11 is also used to decelerate the motor in stopping operations.

When PLAY is pressed, a low play command logic signal is routed to the preset or clear input of play direction flip-flop U50-8/9, depending on whether play direction switch S1-3 on the capstan PWA is set to forward or reverse. If forward, a high is routed to gate U10-12 and a low is routed to gate U18-12 of direction command gates U10-12/U7-11/U18-12/U7-8 from pin 9 and 8 output of U50 respectively. The resulting low from gate U7-8 of the command gates is applied to acceleration transistor, turning it on. At the same time, logic from underspeed latch U18-6/U34-6 and play command (PLC) logic from play latch U30-6/12 is combined at the output of AND gate U26-3 to turn on acceleration switch Q20. As a result, +5V is routed through Q11 and Q20 to provide constant drive to the capstan motor as it comes up to speed.

If play direction switch S1-3 is set to reverse, the logic level from gate U7-8 will be high. Acceleration transistor Q11 will then have been kept off and -5V will be routed through acceleration switch Q20 to accelerate the motor in the reverse direction.

It was described earlier that when the capstan motor comes up to speed, phase-lock flip-flop U33-6, U33-11 of the phase comparator toggles to provide a phase-

modulated error signal which is routed through carrier filter U57-1, compensation amplifier U58-1, and phase-lock switch Q21 to control the speed of the capstan motor. Also described was how the toggling of U33-6/U33-11 resets underspeed latch U18-6/U34-6 causing generation of the phase-locked (LKD) logic level, which in addition to being transmitted to the Main CPU and STC PWAs, also causes phase-lock switch Q21 to close and to cause insertion of integrating capacitor C93 in the compensation amplifier. In addition to the above, the resetting of underspeed latch U18-6/U34-6 causes acceleration switch Q20 to open, thereby removing speed control of the capstan motor by acceleration transistor Q14. Direction control is then transferred to direction sense flip-flop U50-5/6 in the phase-locked mode. In the forward direction, tach pulses to the flip-flop cause the output at pin 6 of U50-5/6 to be positive. The positive level is applied to one input of exclusive-OR gate U6-3 to cause the phase-modulate error signal from U33-6, which is run through the other imput of U6-3, to be inverted before being applied to the carrier filter. If direction switch S1-3 is set to reverse, the output level from pin 6 of U50-5/6 will be negative and the error signal through U6-3 is uninverted.

As mentioned in the phase comparator description, overspeed latch U33-8, U34-11 (in the overspeed condition) is set to close the servo channel so that drive in opposition to the capstan motor overspeed may be effected to slow the motor down.

When STOP is pressed, capstan motor drive from acceleration transistor Q11 opposes the direction of motor rotation in order to provide dynamic braking. The low generated through the pressing of STOP is processed through gates U7-3, U7-6, and U44-12 to set stop latch U31-6, U31-8. Logic from the stop latch is then processed through gates U16-3 and U16-6, providing a high-to-one input of stopping logic and gate U12-6. The other input to U12-6 was latched high prior to the pressing of the STOP button so that a low is presented to U10-12 and U18-12 of the direction command gates. Also, direction sense flip-flop U50-5/6 provides a logic high-to-one input of gate U7-11 of the direction command gates if the capstan is rotating in the forward direction and a logic low if rotation is in the reverse direction. Thus if capstan rotation is forward, a logic high appears at the output of gate U7-8. This results in constant reverse drive from acceleration driver Q15 to decelerate the capstan motor. The opposite is true if capstan rotation is sensed by U50-6/7 as being in the reverse direction. In this case, the stop command causes capstan drive in the forward direction to decelerate the capstan motor. When the motor slows to about 0.5 in/s, motion sense one-shot U17-6 resets stopping latch U12-8, U12-11 causing acceleration switch Q20 to turn off.

## 4-24 Reel Servo Cross-Coupling

In the absence of control, differences in the sizes of capstan and reel diameters could cause the capstan to call on a reel to accelerate to the point where excessive tension is imposed on the reel tape, ruining the tape. To prevent this, a compensating velocity/acceleration signal is sent from the reel servo to the capstan MDA via x-couple switch Q19 to reduce capstan drive. This switch is on in underspeed and overspeed conditions providing the servos are armed and PLAY is activated. The switch is also on in all shuttle operations and following the STOP command.

#### 4-25 Shuttle Circuit

The shuttle circuit responds to commands from FAST FWD and REWIND on the machine control panel and from SHUTTLE on the set-up panel. With none of these controls activated, 15V are applied from the emitter of Q16 to the base of Q17 of comparator Q17/U55. This in turn provides about 15V to the inverting input of U55. Because the non-inverting input of U55 is fed a ramp voltage from ramp generator Q13/Q12 which never reaches the level at the inverting input of U55, the shuttle circuit remains inactive.

When REWIND is pressed, a voltage drop across 1.1 resistor R30 causes about 13V to appear at the base of Q17 of the comparator. When FAST FWD is pressed, a voltage drop across 24-Kohm resistor R29 causes about 2V to appear at the base of Q17. When the shuttle touchbar is pressed at a certain point over its length, a voltage corresponding to the point between the 2V and 13V levels appears at the base of Q17. Within the voltage limits described above, the ramp voltage of the ramp generator at the non-inverting input of U55 will at some point exceed that of the value set at the inverting input, causing U55 to switch and activate the tape transport.

In operation, 6-bit counter U36/U38, consisting of cascaded 2-bit counter U36 and 4-bit counter U38, is clocked by the 9600-Hz reference frequency from the VSO PWA. After a count of 64 the counter is reset and provides a carry-out to the base of Q12 which results in the quick discharge of the ramp voltage charge buildup on capacitor C85. The carry is also applied to the input of shift register U61. After 192 pulses are counted, during which time three ramp voltages are generated and three carry inputs to shift register U61 are generated, U61 provides an enabling input to AND gate U21-3.

The other input to AND gate U21-3 is generated following a fourth ramp buildup when the ramp level at the non-inverting level of U55 just exceeds the switch level at the inventing input. At that level U55-7 goes positive causing one shot U60-13 to trigger. This causes the output of AND gate U21-3 to generate a positive pulse for 200 µs. The positive pulse clocks the input of latch U37 which is the output of 6-bit counter U36/38 into the output of U37. The output of U37 is a digitized representation of the ramp analog voltage at the time of U55-7 switching and corresponds to the INPUT pushbutton or SHUTTLE touchbar switching level.

Debouncer one-shot U60-5 is triggered for 150 µs following each ramp when the output at U55-7 goes low. Its operation is significant during the generation of every fourth ramp when AND gate U21-3 is enabled by shift register U61. During the fourth ramp buildup one-shot U60-13 is held inoperative by the debouncer for 150µs, preventing U60-13 from being triggered by random transients which could occur during that period.

The output of latch U37 is applied to a D/A counter consisting of op-amp U56-6 and input scaling resistors. The reconverted analog output is routed through shuttle switch Q19 and then through the MDA to the capstan motor. The output pulse from AND gate U21-3 which clocks latch U37 also sets shuttle latch U31-12, U30-8 which in turn causes shuttle switch Q19 to turn on (SHC logic).

During shuttle operations the MDA is turned into a voltage mode amplifier by the feedback through resistor R142 to the input. This allows greater velocity control over the capstan motor than with a current mode amplifier.

### 4-26 Near-End-of-Tape Stopping Circuit

The near-end-of-tape stopping circuit provides that as the tape approaches the point of winding off the reel in either direction in a shuttle mode (or fast forward or rewind), the circuit will either cause the transport to stop, preventing the tape from completely winding off the reel, or reduce operation to play speed as the tape winds off the reel. The choice depends on the setting of play off/stop switch S1-1 on the PWA.

The circuitry involved includes divide-by-100 counter U1/U2 consisting of two cascaded divide-by-10 counters, two divide-by-2 counters U19 and U3, and near-end stop latch U43-8, U43-12. The divide-by-100 counter counts the capstan tach-rate pulses while the divide-by-2 counters U19 and U3, respectively, count the varying rate takeup and supply reel pulses. Before the end-of-tape stopping point is reached, the reel tach rate of the reel being unwound will have a one or less pulse output for every 100 pulses from the capstan tach. Under this condition, only the first stage of the divide-by-2 counter of interest will at most be set by any reel tach pulse before 100 pulses are generated by the capstan tach; then, at the generation of 100 capstan tach pulses, the divide-by-two counters are cleared.

On the other hand, at the end-of-tape stopping point, the unwinding reel tach rate will be high enough to generate a second tach pulse before 100 capstan tach pulses are generated. The first reel tach-rate pulse will cause the first stage of the divide-by-2 counter of interest to be set, while the second one will cause the second stage to be set. The output of this second stage will then be combined with the shuttle command logic (SHC) so that near-end-of-tape stop latch U43-8, U43-12 will be set. If play/stop switch S1-1 is set to stop, the low from U43-12 will set stop latch U31-6, U31-8 and the stop (STC) command will be generated. If the play/stop switch is set to play, the low from U43-12 will be applied to play flip-flop U30-6, U30-12 to activate the play command (PLC) and to the clock input of play direction flip-flop U50-8/9 to clock the direction logic at the D input into the output. The output of U50-8/9 will then be applied to direction command gates U10-12/U7-11/U18-12/U7-8 for direction logic evaluation and the tape will run off the reel at the play speed.

#### 4-27 FET Switch Control

Table 4-3 summarizes the state of the FET switches discussed in previous paragraphs under the various modes of operation.

## 4-28 Reel Servo Functional Description

The reel servo is a closed-loop servo that controls the reel motors to maintain constant tape tension across the heads in all modes of operation. Figure 4-7 is a simplified block diagram of the reel servo system.

The reel servo is not concerned with how much tape is on a reel (as in an open-loop reel servo) but only with the tape tension on either side of the capstan. These

Table 4-3. Capstan Servo FET Switch Control

Servo Condition	Integrator Bypass Switch Q14	Phase Lock Switch Q21	Acceleration Driver Switch Q20	X-Couple Switch Q18	
Underspeed	On	Off	On	On	
Overspeed	On	Off	On	On	
Phase Locked	Off	On	Off	Off	
Stopped	On	Off	Off	Off	

tensions are sensed by position of the tension arms and must be near equal in all modes of operation. The tension arms are positioned by the tape and all tape motion is controlled by the capstan. The reel servo controls the supply and takeup of tape based on information the servo receives from the tension arm sensors. Actual value of tape tension is controlled by the takeup and supply reel motors. The force provided by the spring-loaded tension arms is opposed by the force supplied from the reel motors through the tape. From the springs and tension offset, the tape tension value depends on a given operating condition. When the reel servo is activated (tape threaded and taut), reel motors are activated.

If tape tension varies during operation, the tape tension arm is moved off position. This change in position is sensed by means of a ferrite I-bar on the arm assembly and an E-core transformer on a Supply and Takeup Position Adjustment PWA. The position output signal is a voltage proportional to arm position and is the servo error which adjusts the drive to the appropriate reel motor to maintain proper tape tension.

The servo error voltage, which is amplified and compensated for the mechanics of this system, modulates a 28.8-kHz carrier frequency to develop a pulse-width modulated (PWM) signal with a duty cycle that varies with the magnitude of the servo error signal. The PWM signal is fed through a gate, which is enabled by the servos-on logic, routed to a dual-polarity class D motor drive amplifier driver, and amplifed from a TTL level signal to a level suitable for driving the motor drive amplifier (MDA) switching transistors. The switching transistors alternately switch positive and negative, approximately 35 Vdc (70 Vp-p), across the motors at a 28.8 kHz rate. As a result of the dc motor inductance, the 28.8-kHz signal and its harmonics are filtered and only the dc component of the current remains significant. Motor torque is proportional to the current applied to the motor. When the duty cycle is exactly 50%, the dc current in the motor is zero and the motor has no torque.

#### 4-29 Reel Servo Circuit Details

The reel servo circuitry is principally located on Reel Servo, Position Adjustment, and Offset Adjustment PWAs, and on the transport assembly. Figure 4-8 is a simplified block diagram of the reel servo (Schematic No. 4840472, 4840499, 4840480).

### 4-30 Takeup and Supply Tension Sensors

Tension arm position is sensed by motion of a ferrite bar on the arm assembly and an E-core transformer on the A Position Adjustment PWA. Motion of the arm assembly relative to the E-core transformer causes a voltage to be sensed, corresponding to the position of the tension sensor arm. The total voltage range is approximately +2.0 to -2.0 Vdc when the arm is moved from one extreme to the other. Under actual servo conditions, the voltage may change only a few tenths of a volt. When the recorder is in the armed condition, the force on the tension arms from the reels (through the tape) is balanced by the torque exerted by the tension arm springs.

### 4-31 Takeup/Supply Position Adjustment

The takeup and supply position adjustment circuits are similar; therefore only the takeup position adjustment is discussed. Refer to block diagram Figure 4-8 and Schematic No. 4840480 for this discussion.

A 57.6-kHz clock signal is routed from the master clock through amplifier Q6, Q7 on the Offset Adjustment PWA to takeup tension sensor T1 on the Takeup Position Adjustment PWA. This signal provides input for transformer T1. The input and output signal from T1 goes to precision half-wave rectifier U1-1, is filtered by capacitor C6, and is then amplified by buffer amplifier U1-7 which has a position adjust, R3, to compensate for any lateral positioning error of the I-core relative to the E-core. The output of amplifier U1-7 is the takeup tension error and is routed through buffer U1-1 on the Offset Adjustment PWA to the Reel Servo PWA.

If the tension arms swing too far in toward center, the error voltage generated by the tension arm sensor exceeds a preset reference level (set by limit adjust R34) and comparator U2 provides an output signal to gate U3. This limit signal (SVA) is routed to the capstan/transport control PWA and shuts off the servo. Situations where the tension error limit can be exceeded include:

- End of tape has run off the reel.
- Tape has broken.
- There is a loss of transport or servo control.

Indicator DS1 on the Takeup Position Adjustment PWA illuminates when the tension is exceeded.

If the tape is stopped, both arms are in an equivalent position and there is equal tension at the arms. If tape is moving, the arm that is on the side of the transport taking up tape (not necessarily the takeup arm) should have a higher tension to make up for friction losses across the tape path. To accomplish this, an offset voltage is injected into the tension arm error signal. This voltage makes the reel servo for the side of the transport taking up tape want to have a higher torque, i.e., it runs with the tension arm further out.

In compensating for the frictional losses across the tape path, the motion sense and true direction (TDR) logic signals from the Capstan Servo/Transport Control PWA

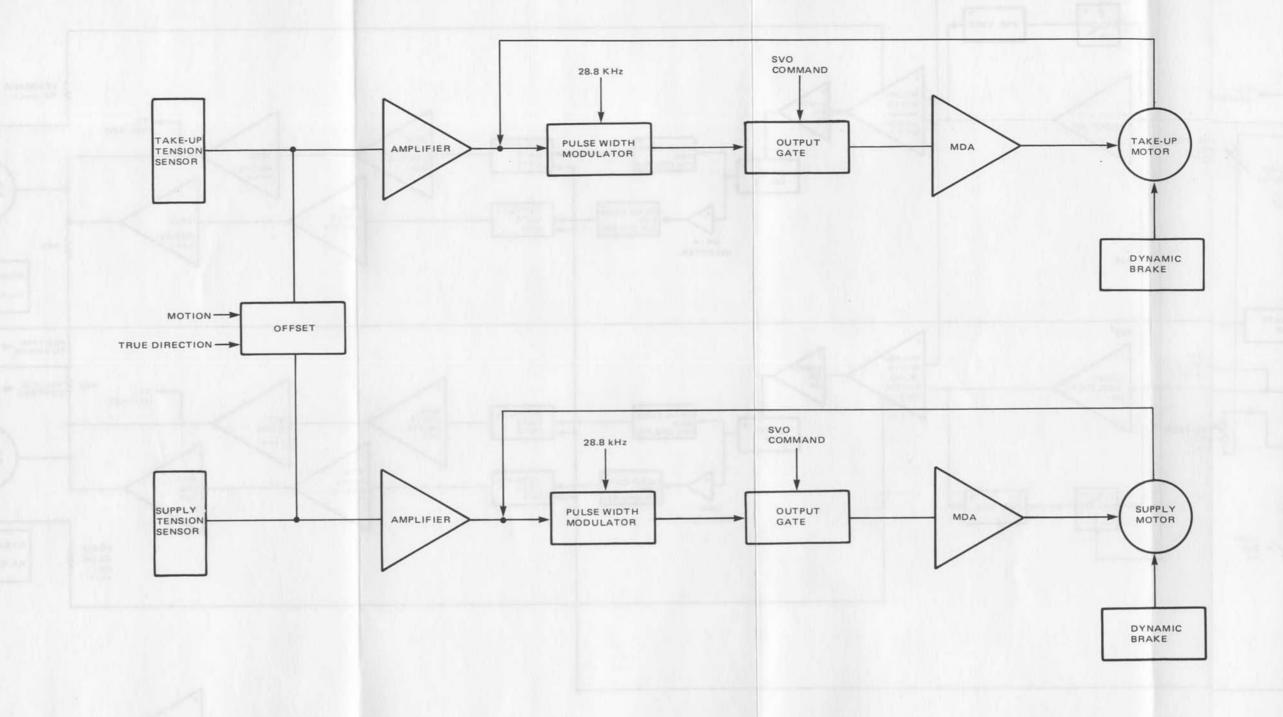
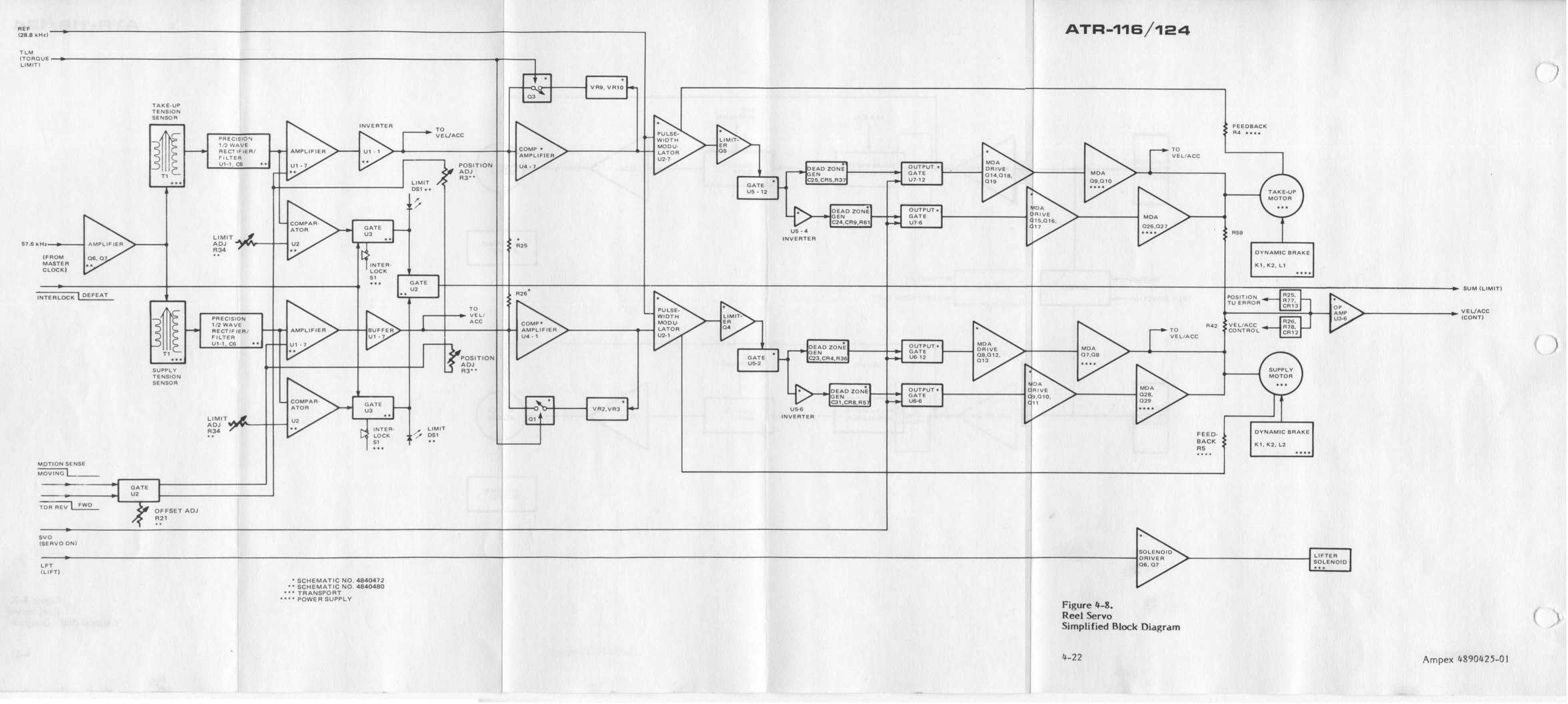


Figure 4-7. Reel Servo General Block Diagram



are routed to gates U2-11, 6, and 8 on the Offset Adjustment PWA. If the TDR signal is low, the output of gate U2-8 is low and Q4 will be off. This enables the positive offset voltage, adjustable through offset adjust R21, to be routed to the inverting input of buffer U1-7 on the Takeup Position Adjustment PWA. This results in a higher tension position on the take-up position arm. Similarly, if the supply side reel is actually taking up tape, the TDR signal is high. Q5 is then off and the offset adjust voltage is routed to the inverting input of buffer U1-7 on the Supply Position Adjustment PWA so that the supply position arm receives more tension.

The take-up error signal from U1-1 of the Offset Adjustment PWA, as indicated above, and also the supply error signal from the same PWA, are routed to respective amplifiers on Reel Servo PWA. The takeup signal is inverted. The two signals are, therefore, of opposite polarity and under most conditions the reel motors do not run on the same power supply, i.e., one reel motor runs on the positive 35V power supply while the other runs on the negative 35V power supply. This results in a more balanced power supply operation.

### 4-32 Compensation Amplifier

The takeup and supply reel servos are similar in operation; therefore, only the takeup reel servo is described. The output dc voltage (error signal) from the Offset Adjustment PWA is routed to feedback compensation amplifier U4-7 (Schematic No. 4840472). The feedback compensation amplifier provides gain for the error signal and together with R4, C2, and R3 provides compensation for the mechanical properties of the transport. When tape is threaded on the transport prior to initiation of the thread mode, the tension arms are held by spring tension in the parked position. This results in a large servo error when the servo is activated. For operator safety when the reel servos are activated, the range of the compensation amplifier is temporarily reduced. This is the limited torque servo condition (before any transport mode is entered). A logic low torque limit command (TLM) from the Capstan/Transport Control PWA causes FET switch Q3 to turn on and increase the feedback around amplifier U4-7 (if the output is above 4V). This reduces the amplifier output range as determined by the voltage drop of voltage regulators VR9, VR10. After the limited torque servo condition is obtained, the servo is engaged and any transport mode is activated, the torque limit command is removed and full range is restored.

#### 4-33 Pulse-Width Modulator

The amplified and compensated signal from feedback amplifier U4-7 is used to modulate a 28.8-kHz carrier signal from the VSO PWA. These two signals are applied to the summing (inverting) input of pulse-width modulator (PWM) U2-7. The high-frequency integrating characteristics of the modulator produce a triangular waveform summed with the error signal from amplifier U4-7 (see waveform Figure 4-9). The composite signal is applied to amplifier/limiter Q5 that amplifies and clips the signal to produce a rectangular waveform with transitions corresponding to the zero crossings of the summed signals. The rise time of the rectangular waveform is decreased by gate U5-12 and results in a clean waveform occurring at a 28.8-kHz rate with a duty cycle that is a function of the error signal. When there is zero servo error, the duty cycle is 50% and the reel motors stand still.

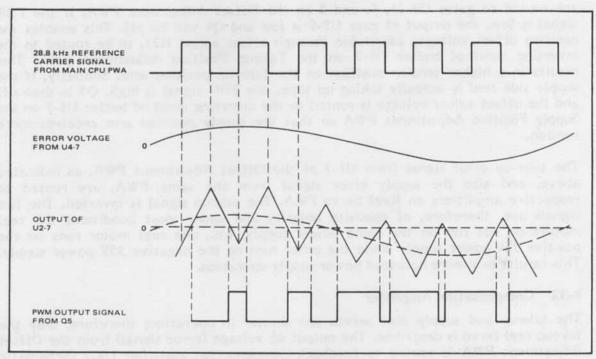


Figure 4-9. Pulse Width Modulator Waveforms -Takeup Reel Servo

### 4-34 Output Gates and MDA

The pulse-width modulator signal from U5-12 is fed to the input of output gate U7-12 and through inverter U5-4 to output gate U7-6 to produce two 180° out-of-phase MDA signals. The MDA is a switching type power amplifier. A residual charge remains on the base of the switching transistors after the drive signal has turned off and therefore the transistors do not turn off instantly.

Thus, without correction, it is possible that opposite polarity MDA transistors can be on at the same time and cause overheating of the output switching transistors (Q9, Q10, Q26, Q27). To prevent this condition, the signal from U5-12 is also fed to dead zone generator R37/CR5/C25 and through U5-4 to dead zone generator R61/CR9/C24. The generators modify the PWM signals, and the modified and unmodified signals are combined in gates U7-12 and U7-6 to produce an MDA drive signal with a dead zone as shown in Figure 4-10. The dead zone allows time for the base junction to discharge.

The takeup and supply reel servos are turned on by the logic low reel servo on command from the Capstan/Transport Control PWA. The logic low is inverted by gate U1-8 and enables gates U6 and U7. When gates U7-12 and U7-6 are enabled, opposite phase 28.8-kHz drive signals are fed through the MDA drive transistors (Q14/Q18/Q19 and Q15/Q16/Q17) to MDA switching transistors Q9/Q10 and Q26/Q27 located in the heat sink area. The transistors are alternately switched on and off to provide a +35V and -35V drive across the reel drive motor. Refer to Figure 4-10. Switching transistors Q9/Q10 or Q26/Q27 conduct when the output at U7-12 or U7-6, respectively, is in a low state.

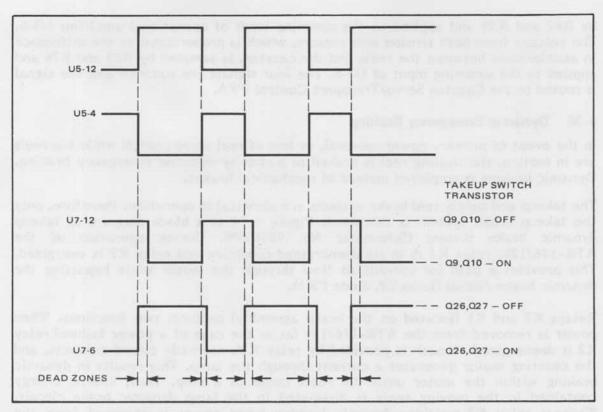


Figure 4-10. Dead Zone Generator Operation and MDA Switch Transistor Conduction State

The current of the drive motor is sampled across a  $0.1\,\Omega$  resistor R4 located in the power supply. The dc component of the sampled signal provides feedback and is applied to the inverting summing input of pulse-width modulator U2-7 to enable the modulator/MDA to be a current source for the motor. For any given error voltage, the feedback provides for constant motor torque at all operating speeds.

### 4-35 Velocity/Acceleration Control

During capstan servo underspeed and overspeed condition, braking, and shuttle modes of operation, a velocity/acceleration control signal is developed on the Reel Servo PWA. This signal is routed to the Capstan Servo/Transport Control PWA to slow the acceleration or velocity of the capstan motor. For example, the capstan may require the reel motors to turn faster than the available reel motor torque permits.

The velocity/acceleration control circuitry senses this and generates an analog voltage that is used to prevent the capstan from turning faster than allowed by the reel size. Similarly, the velocity/acceleration control signal prevents the capstan motor from accelerating faster than the reel motors can accelerate due to varying reel sizes.

The velocity/acceleration control signal is developed as follows. The dc voltage developed across the reel motors, which is proportional to reel velocity, is sampled

by R42 and R59 and applied to the summing input of operational amplifier U3-6. The voltage from both tension arm sensors, which is proportional to the difference in acceleration between the reels and the capstan, is sampled by R25 and R26 and applied to the summing input of U3-6. The four signals are summed and the signal is routed to the Capstan Servo/Transport Control PWA.

#### 4-36 Dynamic Emergency Braking

In the event of primary power removal, or loss of reel servo control while the reels are in motion, the trailing reel is braked to a stop by dynamic emergency braking. Dynamic braking is employed instead of mechanical brakes.

The takeup and supply reel brake systems are identical in operation; therefore, only the takeup brake system is discussed. Figure 4-11 is a block diagram of takeup dynamic brake system (Schematic No. 4840499). During operation of the ATR-116/124, relay K1 is in its deenergized condition and relay K2 is energized. This provides a path for current to flow through the motor while bypassing the dynamic brake circuit (lamp L2, diode CR1).

Relays K2 and K1 (located on the brake assembly) perform two functions. When power is removed from the ATR-116/124 (as in the case of a power failure) relay K2 is deenergized. A path is provided by relay K2's normally closed contacts, and the coasting motor generates a current through the lamp. This results in dynamic braking within the motor until the reels come to a stop. Thus, kinetic energy contained in the moving reels is dissipated in the lamp dynamic brake circuit. Whereas relay K2 provides dynamic braking when power is removed from the ATR-116/124, relay K1 removes the motors from the circuit should the servo on command be absent.

This high logic signal is used to energize relay K1 via transistors Q2, Q3, Q6. Energizing relay K1 opens its normally closed contacts, removing current from the motor, and closes its normally open contacts, loading the motor. Thus, the motors are electrically removed from the MDA circuit, and dynamically braked when the end of tape is reached or if there is tape breakage.

#### 4-37 Lifter Solenoid

A lift command is routed from the Capstan/Transport Control PWA to the Reel Servo PWA. This command turns on driver Q6, Q7 and current flows through the solenoid winding. The transport-mounted solenoid is thereby actuated and the tape lifters moved in and out accordingly.

#### 4-38 Panel CPU

The panel CPU is used to send keyboard command signals to the main CPU for processing and to receive from the main CPU update information for the 270-LED lamp display of the panel. The panel CPU (Figure 4-12 and Schematic No. 4840589) is comprised of a membrane switch panel overlaid on an LED lighting panel which in turn is overlaid on a panel containing integrated circuit (IC) components. These IC components include an 8085A microprocessor (U3), an address decoder (U9), two RAMs (U6 and U24), an EPROM (U13), a universal asynchronous receiver/transmitter (UART) (U7), five 8279 programmable keyboard/panel display interface

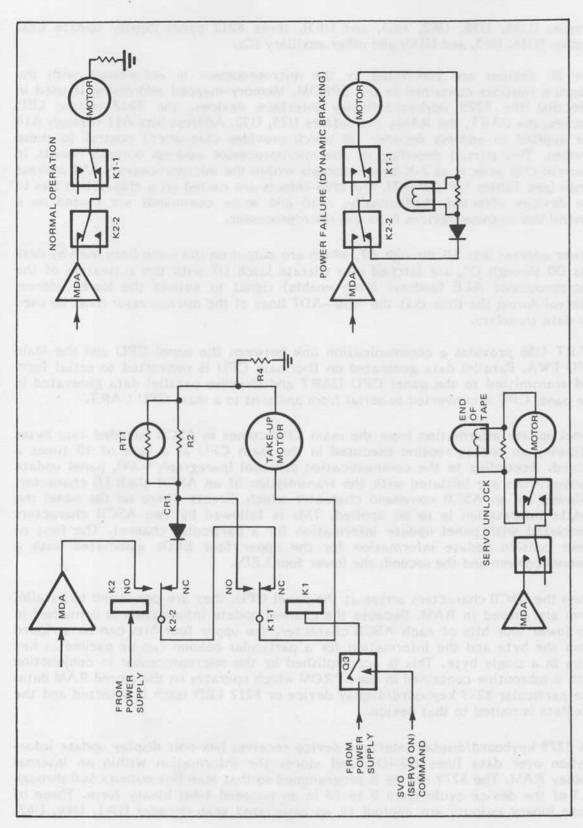


Figure 4-11. Takeup Dynamic Brake-Block Diagram

devices (U56, U58, U62, U63, and U65), three 8212 panel display update LED latches (U14, U15, and U16), and other auxiliary ICs.

The IC devices are controlled by the microprocessor in accordance with the program routines contained in the EPROM. Memory-mapped addressing is used in selecting the 8279 keyboard/display interface devices, the 8212 update LED latches, the UART, the RAMs and buffers U25, U32. Address bits All through Al4 are applied to address decoder U9 which provides chip-select control to these devices. This partial decoding of the microprocessor address outputs results in discrete chip selects at 2-K-byte intervals within the microprocessor's 65K address range (see Tables 4-4 and 4-5). The chip-selects are routed on a chip-select bus to the devices affected. Additionally, read and write commands are routed on a control bus to these devices from the microprocessor.

Lower address bits A0 through A7, which are output on the same lines used by data bits D0 through D7, are latched into tristate latch U7 with the activation of the microprocessor ALE (address latch enable) signal to extend the lower address interval during the time that the AD0—AD7 lines of the micropressor must be used for data transfers.

UART U56 provides a communication link between the panel CPU and the Main CPU PWA. Parallel data generated on the main CPU is converted to serial form and transmitted to the panel CPU UART and likewise parallel data generated in the panel CPU is converted to serial from and sent to a main CPU UART.

Panel update information from the main CPU comes in ASCII encoded data bytes following an update routine executed in the main CPU at a rate of 10 times a second. According to the communication protocol (paragraph 4-44), panel update transmissions are initiated with the transmission of an ASCII slash (/) character, followed by an ASCII command character which directs where on the panel the update information is to be applied. This is followed by two ASCII characters associated with panel update information for a particular channel. The first of these contain update information for the upper four LEDs associated with a channel column and the second, the lower four LEDs.

When the ASCII characters arrive at the panel CPU, they are converted to parallel form and stored in RAM. Because the channel update information is contained in the lower four bits of each ASCII character, the upper four bits can be stripped from the byte and the information for a particular column can be packed as hex pairs in a single byte. This is accomplished by the microprocessor in conjunction with a subroutine contained in the EPROM which operates on the stored RAM data. The particular 8279 keyboard/display device or 8212 LED latch is selected and the hex data is routed to that device.

An 8279 keyboard/display interface device receives hex-pair display update information over data lines D0-D7, and stores the information within an internal display RAM. The 8279 device is programmed so that scan line outputs SL0 through SL3 of the device cycle from 0 to 15 in an encoded 4-bit binary form. Three of these binary outputs are applied to an associated scan decoder (U41, U44, U47,

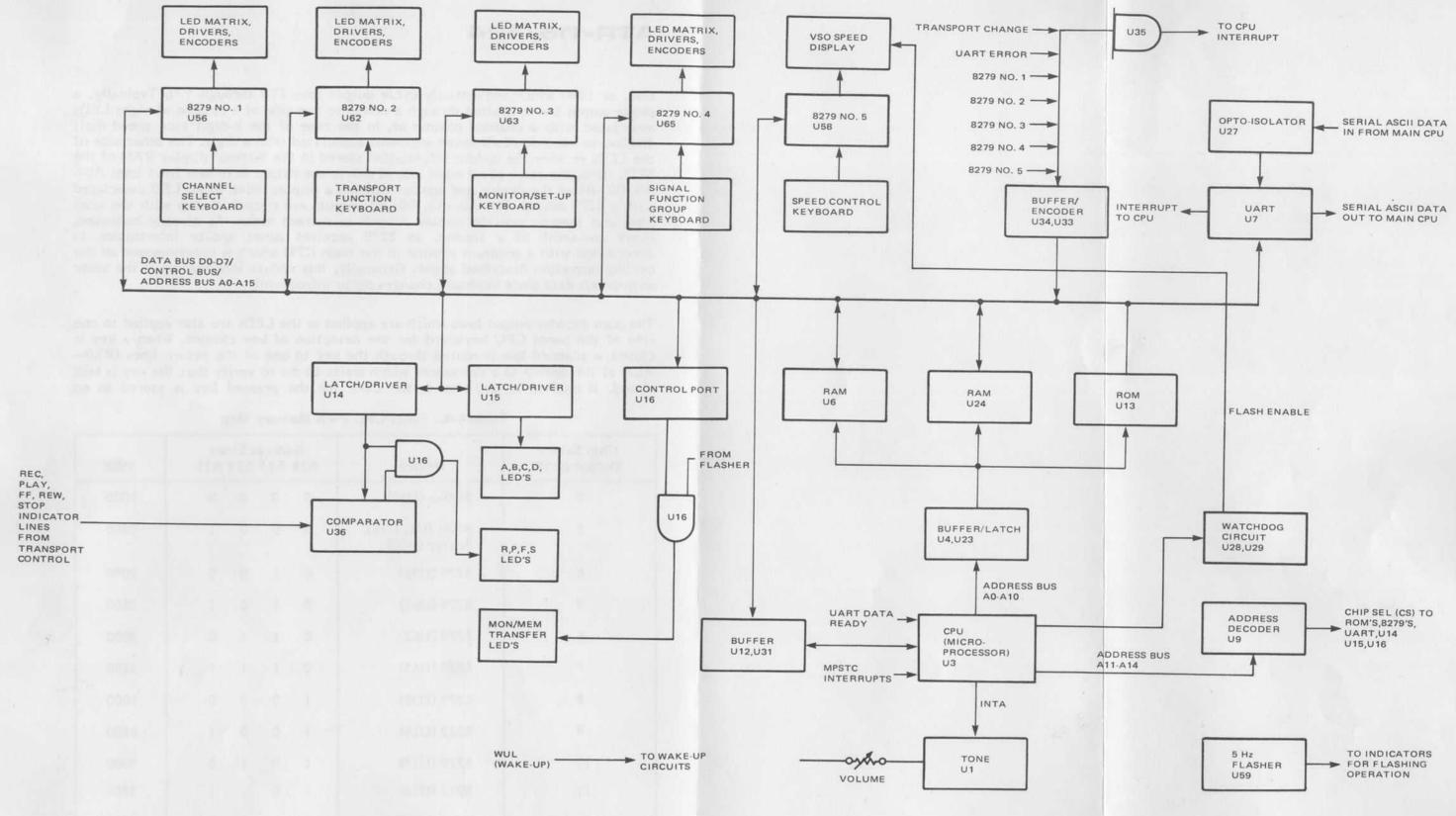


Figure 4-12. Panel CPU Simplified Block Diagram

U50, or U54) which sequentially cycle output lows (Y0 through Y7). Typically, a single output low is applied through a driver to one side of a column of eight LEDs associated with a channel column or, in the case of the 4-digit tape speed digit display, to one side of all seven segments associated with a digit. The other side of the LEDs receive the update information stored in the internal display RAM of the 8279. Here, the state of all eight bits of a byte are output in unison from lines A0—A3, B0—B3 of the device and applied through a display drive to all LED associated with a 8279 device. The A0—A3, B0—B3 outputs are cycled in step with the scan lines and thereby provide display refresh in correct order. As already indicated, every one-tenth of a second, an 8279 receives panel update information in accordance with a program routine in the main CPU which is superimposed on the cycling operation described above. Generally, this update information is the same as previous data since keyboard changes occur infrequently.

The scan decoder output lows which are applied to the LEDs are also applied to one side of the panel CPU keyboard for the detection of key closure. When a key is closed, a scanned low is routed through the key to one of the return lines (RL0—RL7) of the device to a debouncer which waits 10 ms to verify that the key is still closed. If the key is still closed, the code for the pressed key is stored in an

Table 4-4. Panel CPU PWA Memory Map

Chip Select Output of U9	Device	A A14	HEX			
0	Buffer (U32)	0	0	0	0	0000
1	RAM (U6, U24), Buffer (U25)	0	0	0	1	0800
4	8279 (U56)	0	1	0	0	2000
5	8279 (U62)	0	1	0	1	2800
6	8279 (U63)	0	1	1	0	3000
7	8279 (U65)	0	1	1	1	3800
8	8279 (U58)	1	0	0	0	4000
9	8212 (U14)	1	0	0	1	4800
10	8212 (U15)	1	0	1	0	5000
11	8212 (U16)	1	0	1	1	5800
14	UART (U7)	1	1	1	0	7000
15	UART (U7)	1	1	1	1	7800

Table 4-5. Setup Panel PWA Chip Select Functions

Chip Select Output of U9	Device	Function				
0	Buffer (U32)	Combined with RD from 8085 (U3) to enable transfer of data from ad- dressed EPROM (U13) to 8085.				
denie a redail	RAM (U6, U24), Tristate Latch (U25)	For U6, U24 is combined with WR from 8085 (U3) for the temporary (U25)storage of characters received and transmitted by the UART (U7). For U25, is combined with RD to read contents of RAMs (U6, U24) into 8085 (U13).				
4-8	8279 (U56, U62, U63, U65, U58)	Combined with other control signals to 8279 devices to 8279 devices (C/D, (C/D, IRO, WR, RD) to program 8279s, to receive control signals for indicators associated with channel select functions of set-up panel, and to transfer key-board command signals of setup panel for processing in the Main CPU PWA.				
9-11	8212 (U14, U15, U16)	Combined with WR from 8085 (U13) to control state of indicators associated with setup and monitor functions.				
14-15	UART	For serial transmission of data to Main CPU PWA, CS14 is first ANDed with WR to load a parallel data word into trans-mitter register of UART. For reception by the 8085 of a parallel data word serially received from Main CPU PWA, CS15 is ANDed with RD.				

output RAM and the interrupt request line of the 8279 device goes high. The interrupt signal is applied to the interrupt input of the microprocessor which then completes its current instruction cycle and sends an interrupt acknowledge signal (INTA) to the enabling inputs of tristate buffer U33. U33 receives the output of decoder U34 which receives the individual interrupt request signals from the 8279 devices. Encoder U34 encodes the particular interrupt signal with an interrupt vector address. The address is applied through the enabled tristate buffer U33 and to the data D3, D4, and D5 inputs of the microprocessor.

The micropressor then executes the subroutine for sending the keyboard command to the Main CPU. The keyboard coded command is read in from the 8279 device output memory and a series of ASCII characters are generated in accordance with the transmit communication protocol (paragraph 4-44) and stored in RAM (U27/-U28). A sending routine is then called which causes the RAM contents to be loaded into the UART and serially transmitted to the Main CPU UART.\*

#### 4-39 Watchdog Circuit

The panel watchdog triggers if normal execution of the program halts. This causes a local reset and the VSO display will flash. Execution will resume with the VSO display flashing. The flashing can be reset by use of the manual wakeup switch. Recurrence of watchdog triggering indicates a hardware fault.

#### 4-40 Tone/Flasher

The panel CPU contains a tone circuit and a flasher circuit. The flasher is a simple relaxation oscillator that pulses a flash line. The CPU connects this line to indicators to be flashed when a condition, requiring it is encountered.

The tone circuit gives a beep when a keyboard button is pressed. This provides positive indication of the button operation. Pressing a button generates an interrupt to the CPU. The CPU then sends an interrupt acknowledge which is a narrow pulse. This pulse is routed to a dual timer. The first half of the timer is a pulse stretching one-shot. The stretched pulse keys the second half of the timer which is an oscillator and which generates the tone.

#### 4-41 Main CPU

The main CPU (Schematic No. 4840543 and Figure 4-13) receives and processes keyboard command signals from the panel CPU to provide channel-select and function-select signals to as many as three Audio Control PWAs, each of which in turn controls operation of up to eight individual channel Audio PWAs. The Main CPU processes tape speed commands from the panel CPU, and outputs speed select signals directly to the Capstan Servo and Transport PWAs in one of the three fixed tape speed modes; it also outputs indirectly to the capstan servo via the Variable Speed Oscillator (VSO) PWA in the variable tape speed mode. The Main CPU also echoes panel update information to the Panel CPU in response to the signal and speed control commands from the panel CPU. The main CPU is comprised of:

- 8085A microprocessor (U18) and three EPROMs (U25-U27) for processing data.
- CMOS memory array (U31/U33/U35/U36/U37/U40/U42/U44/U45/U46) for storing up to four individual panel CPU setups of 24 channels each.

<sup>\*</sup>When a panel key is closed, the key encoder encodes the keyboard characters in 10-20 ms, allowing for the encoder's debounce time of 10 ms. Control by a computer via the remote connnector will bypass this delay. The dominant delay will then be that of the serial data rate. At the ATR-116/124's normal 19200 baud rate, and using a 10-character word, it takes 1.5 ms to send three ACSII characters.

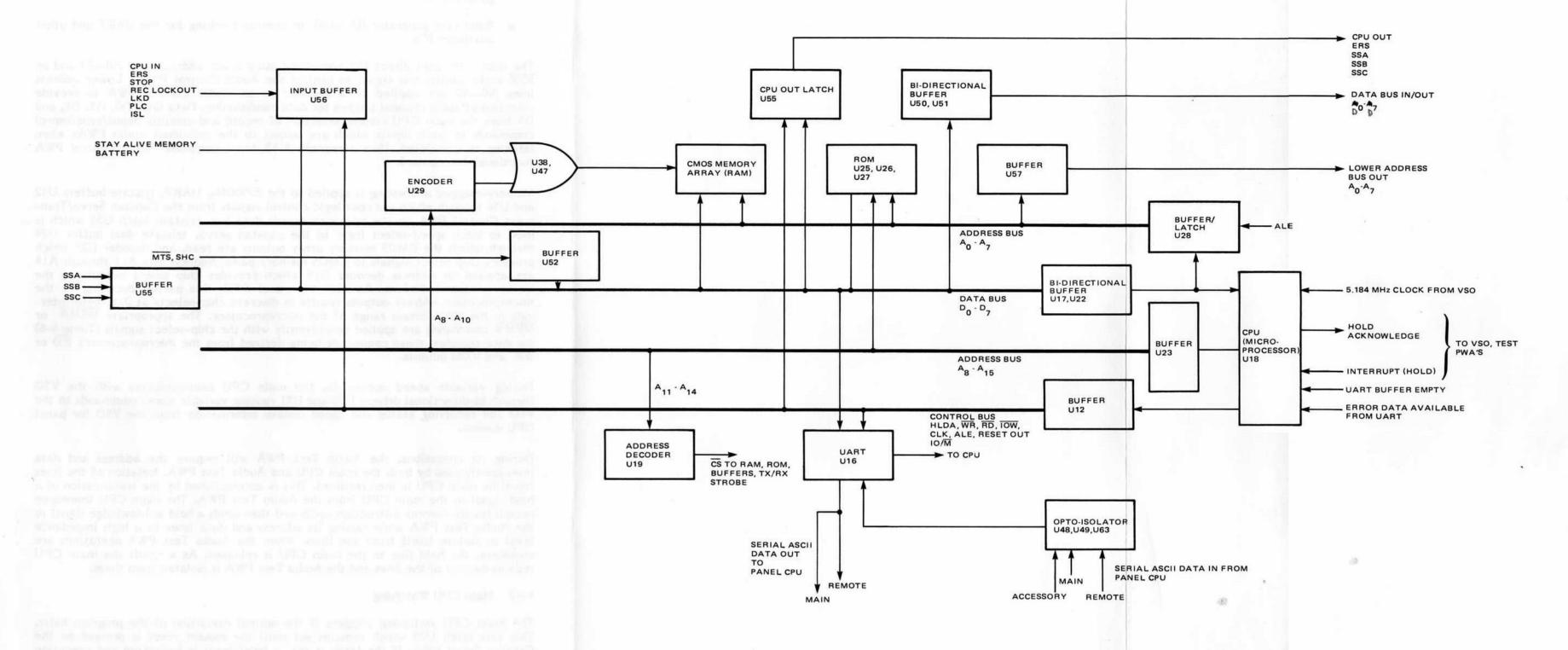


Figure 4-13. Main CPU Block Diagram

- UART (U16) for serially transmitting and receiving data to and from the panel CPU.
- Baud rate generator (U1-U4), to provide clocking for the UART and other auxilliary ICs.

The main CPU uses direct I/O addressing using lower address lines A0—A7 and an IOW write control bus signal to control the Audio Control PWAs. Lower address lines A0—A7 are applied to a decoder on an Audio Control PWA to provide selection of audio channel latches for data conditioning. Data lines D0, D3, D4, and D5 from the main CPU convey selection of record and monitor (input/sync/repro) commands to latch inputs which are output to the individual Audio PWAs when latching is completed. (See paragraph 4-48 for a complete Audio Control PWA functional description).

Memory-mapped addressing is applied to the EPROMs, UART, tristate buffers U52 and U56 through which are read logic control signals from the Capstan Servo/Transport Control PWA on the microprocessor's data bus, tristate latch U55 which is used to latch speed-select logic to the capstan servo, tristate dual buffer U24 through which the CMOS memory array outputs are read, and decoder U29 which provides chip select signals to CMOS memory pairs. Address bits A11 through A14 are applied to address decoder U19 which provides chip select outputs to the memory-mapped devices. As with the panel CPU, this partial decoding of the microprocessor address outputs results in discrete chip-selects at 2-K-byte intervals in the 65K address range of the microprocessor. The appropriate MEMR or MEMW commands are applied concurrently with the chip-select signals (Table 4-6) for data transfer, these commands being derived from the microprocessor's RD or WR and IO/M outputs.

During variable speed operations, the main CPU communicates with the VSO through bi-directional drivers U50 and U51 routing variable speed commands to the VSO and receiving status and speed update information from the VSO for panel CPU display.

During its operations, the Audio Test PWA will require the address and data lines jointly used by both the main CPU and Audio Test PWA. Isolation of the lines from the main CPU is then required. This is accomplished by the transmission of a hold signal to the main CPU from the Audio Test PWA. The main CPU thereupon completes its current instruction cycle and then sends a hold acknowledge signal to the Audio Test PWA while raising its address and data lines to a high impedance level to isolate itself from the lines. When the Audio Test PWA operations are complete, the hold line to the main CPU is released. As a result the main CPU regains control of the lines and the Audio Test PWA is isolated from them.

### 4-42 Main CPU Watchdog

The main CPU watchdog triggers if the normal execution of the program halts. This sets latch U29 which remains set until the master reset is pressed on the Capstan Servo PWA. If the latch is set, a local reset is generated and execution

will resume. U29 will remain set, causing the record function to be locked out and the fault LED to illuminate. Under these conditions, machine operation can continue but recording is locked out. Persistent illumination of the fault LED after master reset indicates a hardware fault.

Table 4-6. Main CPU Chip Select Functions

Chip-Select	Device	Function				
0-2	EPROMs U25, U26, U27,	CS 0, I, and Z provide chipselects to respective EPROMS U25, U26, and U27. Chip-select is combined with MEMR to read in a particular addressed memory location.				
3	One-of-8 memory pair select (U29)	Enables addressed selector to provid a chip-enable signal (CE2A-CE2H) t read/write memories used in storing recorder system setups.				
4	UART (U16)	ANDed with MEMR to strobe (T <sub>r</sub> ) UART (U16) for inputting data to 808 data to 8085 (U18) serially trans- mitted from panel CPU PWA.				
5	UART (U16)	ANDed with MEMW (WR ·10/M) to strobe (T <sub>X</sub> ) UART (U16) for serial transmission of data to setup panel.				
6	3-state buffer (U56)	Combined with MEMR to input status signals to 8085 (U18) from Capstan Servo PWA (STC, PLC, LKD) Audio Control PWA (ERS), and Setup Panel PWA (RCC, STOP BTN).				
7	3-state buffer (U52)	Combined with MEMR to input status signals to 8085 (U18) Capstan Servo PWA (MTS, SHC).				
8	3-state buffer (U55)	Combined with MEMW (WR · 10/M) to output tape speed select signal to Capstan Servo, STC, and STC, and Audio Test PWAs.				
9	OR gate U58-6 OR gate U58-12	For U58-6 is ANDed with MEMR and for U58-12 is ANDed with MEMW.  In both cases purpose is to strobe handshake line from Main CPU PWA to VSO PWA.				

### 4-43 ATR-116/124 Communications Protocol

Communications between the panel CPU and the main CPU are in serial, ASCII encoded format. Table 4-7 is a chart of ASCII code assignments for numbers, letters, special symbols, and non-printing control characters. The areas not shaded contain the characters used by the ATR-116/124 for communications.

Most Significant Hexadecimal Character Least Significant 7 0 2 3 5 6 1 Hex Character P 0 NUL DLE SP 0 å P 1 SOH DC1 1 A 0 P a 11 2 B R b 2 STX DC2 r S 3 C 3 DC3 ETX C S 4 D T d 4 EDT DC4 + t 5 NAK 96 5 E U ENO u e 6 F V 6 ACK SYN å f 7 G W 7 BEL ETB w g 8 H X 8 CAN h BS X 9 Y 9 I ì HT EM J Z A LF SUB : Z K B VT ESC k : C FF FS < L 1 } CR GS M D = m E SO RS > N Λ n DEL F SI US 0 0

Table 4-7. Hexadecimal ASCII Code Conversion

#### 4-44 Panel CPU to Main CPU Communications Protocol

Table 4-8 lists the sequence of ASCII characters which are routed from the panel CPU to the main CPU when a pushbutton on the panel CPU is pressed. Generation of a command character is followed by either an end of file carriage return or by one or two characters associated with the function and then an end-of-file carriage return. A teletype (TTY) keyboard may be substituted for the panel CPU keyboard. In using a TTY keyboard in selecting a function, the associated command and numerical characters are typed, followed by the sending of an end-of-file carriage return.

#### 4-45 Main CPU to Panel CPU Communications Protocol

A background routine in the Main CPU continuously updates the panel CPU LED displays at a rate of ten times per second. A single updating takes place as the transfer of six blocks of ASCII characters with a 7-ms interval separating each block.

Execution time in the Main CPU runs around 2-5 ms depending on the routine executed. Routines which update the latched drive lines to the panel CPU LED

Table 4-8. ATR-116/124 Communication Protocol (Setup Panel to Main CPU)

Pushbutton	Command Character	Next Character
AUX	A	Carr Ret
ALL	B (Block)	Carr Ret
Channel Select	С	0-2 (tens), then 0-9 (units)
Function:		
REC	F	1
READY	F	2 3
SAFE	F	3
INPUT	F	4 5
SYNC	F	5
REPRO	F	6
MUTE	F	7
GROUP	F	8
Group:		
Gl	G	1
G2	G	2
G3	G	2 3 4
G4	G	
Group Clear	K (Kill)	
MASTER RESET	1 (Initialization)	Carr Ret
TAPE SPEED:	T	
7.5	S. S	Authorization
of 11 15 sames barrens	S S S S S S S S S S S S S S S S S S S	2
30	S	3
VSO		C (C ) - 1
VSO	V	S (Select)
DEC	V	D
INC	V	D (D)
% TONE	V	P (Percent)
areas in the bulleting orders	non World man to game	T politicianos) (1988 s
SETUP MEMORY:	to the second second second	Cit start in, tellmann by
A A Harmonia A A A A A A A A A A A A A A A A A A A	P	se In second , dv
В	P	2 3
C	P	3
D	P	r = 4 mil entreng 1 des

(Continued next page)

Table 4-8. ATR-116/124 Communication Protocol (Setup Panel to Main CPU) (Continued)

Pushbutton	Command Character	Next Character
रक्षी दशकी	- X-1-	- 3/19/
MONITOR MEMORY:	(abnic) 0	3.17
R	М	Chappe) Select
R P	M	2
F	M	2 3
S	M	4
TD 4 1 1 5 T T D		- Yoxas
TRANSFER		0.374
PANEL MEMORY	X	P
MONITOR MEMORY	X	M
REC*PLAY	R	P
REC*PLAY	R	3
REC*REH	R	Н
TRANSPORT		- Square
Buttons:		2
STOP	Т	1 10
PLAY	T	1
FAST (FWD, RWD)	T (III.38) N	2 3
Status line:	and and the	THE RESTRICT
SERVOS UNLKD	Т	4

Note: REC\*PLAY means that RECORD and PLAY have been pressed together. An external controller may use command character R to accomplish the same effect. All characters are ASCII.

displays are block-structured in a way that data for 24 channels is processed even if only one channel actually changes. This means that the time required to implement record, for instance, is always within about 150  $\mu$ s of 4.9-ms RPFS routines are longest, taking about 6 ms to implement.

The ASCII transmission format of each block consists in the following order: An ASCII slash (/), followed by a command character designating the destination of the block, followed by the specific update information, and concluding with a carriage return.

Block 1 provides for the updating of the 24 channel columns, 8 columns under the control of each 8279 keyboard/display interface device U56, U62, and U63. The order of transmission is as follows:

- a. ASCII "/"
- b. ASCII 1
- c. 48 ASCII characters describing 24 channel columns. Two ASCII characters per column are contained in the high and low nibbles of a byte organized as follows with the high nibble executed first:

CROUP	MILTE	DEDDO	SVNC	INIDILIT	SAEE	READY	DEC
MSB		KE KO	31110	M. 10 1	Jill L	KEMPI	LSB

d. ASCII carriage return

Block 2 provides for the updating of the group clear (GC) status, then the six columns associated with the group G1—G4, ALL and AUX pushbuttons, and finally the paralleled seven right- and left-hand function switches, all the above of which are under control of 8279 keyboard/display device U65. The order of transmission is as follows:

- a. ASCII "/"
- b. ASCII 4
- c. 16 ASCII characters describing the group/function block organized as described for group 1.
- d. ASCII carriage return

Block 3 provides for the updating of the speed block LEDs which include the four seven-segment LED speed display and the tape speed and VSO-related pushbutton LEDs all under control of 8279 keyboard/display device U37. The order of transmission is as follows:

- a. ASCII "/"
- b. ASCII 5
- c. Eight ASCII characters describing the four seven-segment speed control digits contained in eight nibbles of four bytes followed by eight ASCII characters also contained in eight nibbles of four bytes (with 26-bit spaces unused) for the visual status of the speed and VSO-related pushbuttons.
- d. ASCII carriage return

Byte organization is as follows:

	BYTE 0							BYTE 7				
ed drive	а	a	a	a	7.5	Jinor			BIT 0			
NIBBLE 2	b	b	b	b	15							
NIBBLE 2	С	С	С	С	30	0.11	Wile-			i	a	i
	d	d	d	d		%				f	g	b
	е	е	e	е			Tone			e	5	0
NIDDI 5 1	f	f	f	f				vso	401		d	
NIBBLE 1	g	g	g	g								
	DP	DP	DP	DP					BIT 7			
	LSD			MSD								

Block 4 provides for the updating of the RPFS monitor LEDs which are controlled through the 8212 panel display update latch U18. The order of transmission is as follows:

- a. ASCII "/"
- b. ASCII 6
- c. Two ASCII characters, the one contained in the lower nibble indicating a selected function.

The selected function accorded a logic 0 (negative logic) as shown in the following illustration in which the R lamp  $(E_H)$  is on:

d. ASCII carriage return

Block 5 provides for the updating of the ABCD monitor memory LEDs which are controlled through 8212 panel display update latch U23. The order of transmission is as follows:

- a. ASCII /
- b. ASCII 7
- c. Two ASCII characters, the one contained in the lower nibble indicating a selected function.

The selected function is accorded a logic 0 (negative logic) as shown in the following illustration in which the  $B LED (D_H)$  is on:

d. ASCII carriage return

Block 6 provides for the updating of the record, rehearse, monitor memory transfer, and setup memory switch LEDs which are controlled through 8212 panel display update latch U17. The order of transmission is as follows:

- a. ASCII "/"
- b. ASCII 8
- c. Two ASCII characters, the one contained in the lower nibble indicating a selected function.

The selected function is accorded a logic (positive logic) as shown in the example of the following illustration in which the RPFS TRANSFER LED (4H) is on:

0 0 1 0 x x x

d. ASCII carriage return

### 4-46 Data/Address Bus

Figure 4-14 is a drawing of the data/address bus in relation to the ATR-116/124 signal and transport control systems.

### 4-47 Variable Speed Oscillator (VSO)

The VSO enables the ATR-116/124 to operate in a variable speed mode. The VSO responds to commands from the main CPU in response to VSO-type keyboard commands on the panel CPU and sends status and panel update information to the main CPU reflecting the actions taken on the VSO. Figure 4-15 is an overall block diagram of the VSO and No. 4840544 is the associated schematic. Figure 4-16 shows the interrelationship of the VSO with other PWAs.

Exchange of data between the main CPU and VSO are controlled through handshake lines VSS and VSI (Figure 4-17) which verify the processing of data before further processing is carried out. In operation, the VSO awaits commands from the main CPU as a result of VSO-related key operation on the panel CPU. When this occurs, the main CPU strobes its VSS line to the VSO informing the VSO that data is available on the data lines (VSD0-VSD7) to the VSO from the main CPU. The VSO responds to the main CPU by strobing its  $\overline{VSI}$  line to the main CPU, which indicates to the main CPU that the VSO is receiving the data. The main CPU then raises its VSS line in response to this. When data is read into the input circuits of the VSO, the VSO VSI line is raised and the main CPU awaits update response over the same data lines from the VSO while the VSO processes the command data from the main CPU; e.g., increase or decrease variable tape speed frequency, change from TONE to %, increment/decrement control, etc. When processing is completed, the VSO strobes its VSI line to the main CPU. This interrupt to the main CPU causes it to strobe its VSS line to the VSO, acknowledging the interrupt. The VSO is then ready to send four bytes of data, each one representing a seven-segment character for the tape speed display on the panel CPU. As each byte is transmitted to the main CPU from the least to the most significant figure, the main CPU strobes its VSS line to the VSO, acknowledging the transmission to permit the VSO to strobe its VSI line and send the next byte.

After a display update, there is a VSO timing command interval during which time the main CPU awaits an interrupt command from the VSO before another display update is processed. This is required when the DEC or INC is held down as it gives the operator the ability of observing the change of display with each update. At the end of the timing interval, the VSO strobes its  $\overline{\text{VSI}}$  line which provides an interrupt to the main CPU. The main CPU strobes its  $\overline{\text{VSS}}$  line in acknowledgement which sets the VSO awaiting another command from the main CPU for the start of another update cycle. The timing interval is set so that display updates are limited to about two to four per second.

The initial command over the  $\overline{VSS}$  line from the main CPU to the VSO, indicating that keyboard data is available, is applied to U26, the 8156 (8155) RAM-I/O ports device. The 8156 has a status register which is interrogated by the microprocessor through a polling routine to provide an indication to the microprocessor when this data is available. The microprocessor then provides a read command to the 8156 which latches the data applied to an I/O port of the 8156 from bidirectional bus

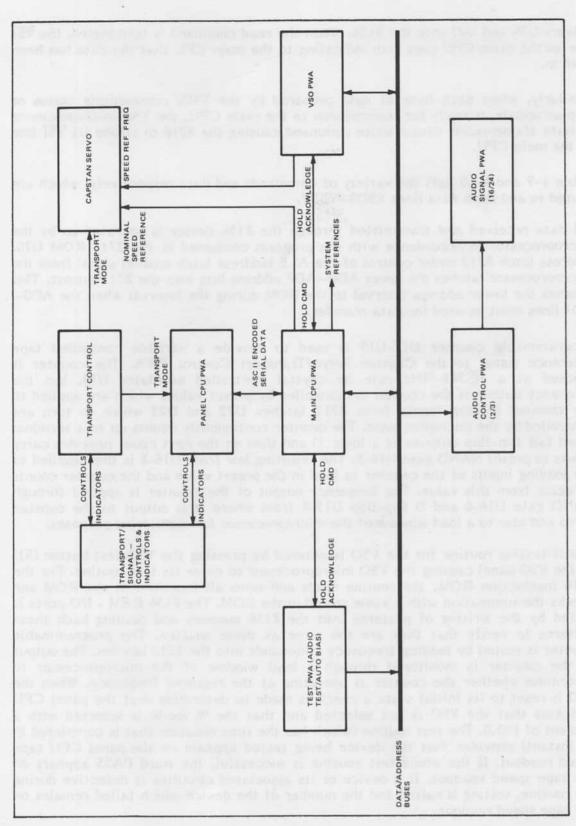


Figure 4-14. Data/Address Bus-Simplified Block Diagram

drivers U24 and U25 into the 8156. When the read command is terminated, the  $\overline{VSI}$  line to the main CPU goes high indicating to the main CPU that the data has been read in.

Similarly, when each byte of data prepared by the VSO, representing status or display update, is ready for transmission to the main CPU, the VSO microprocessor initiate transmission with a write command causing the 8216 to strobe its  $\overline{\text{VSI}}$  line to the main CPU.

Table 4-9 and 4-10 lists the variety of commands and data respectively, which are routed to and from data lines VSD0-VSD7.

All data received and transmitted through the 8156 device is operated on by the microprocessor in accordance with the program contained in the 2716 ROM U20. Address latch 8212 under control of the ALE (address latch enable) signal from the microprocessor latches the lower AD0—AD7 address bits into the 8212 output. This extends the lower address interval to the ROM during the interval when the AD0—AD7 lines must be used for data transfer.

Programmable counter U17-U19 is used to provide a variable controlled tape reference signal to the Capstan Servo/Transport Control PWA. The counter is clocked at a 10.368-MHz rate by crystal controlled oscillator U13, but the frequency output of the counter is controlled by preset values which are applied to the counter loading inputs from 8212 latches U22 and U23 which in turn are controlled by the microprocessor. The counter continuously counts up to a terminal count (all flip-flop outputs at a logic 1) and then on the next count provides carry inputs to preset NAND gate U16-8. The resulting low from U16-8 is then applied to the loading inputs of the counter to load in the preset value and the counter counts up again from this value. The frequency output of the counter is applied through NAND gate U16-6 and D flip-flop U15-8 from where it is output to the capstan servo and also to a load window of the microprocessor for monitoring purposes.

A self-testing routine for the VSO is entered by pressing the VSO test button (S1) on the VSO panel causing the VSO microprocessor to enter its test routine. For the 2716 instruction ROM, the routine reads and sums all locations in the ROM and checks the summation with a value stored in the ROM. The 8156 RAM - I/O ports is tested by the writing of patterns into the 8156 memory and reading back these patterns to verify that they are the same as those written. The programmable counter is tested by loading frequency commands into the 8212 latches. The output of the counter is monitored through a load window of the microprocessor to determine whether the counter is operating at the required frequency. When the VSO is reset to its initial state a check is made to determine that the panel CPU indicates that the VSO is not selected and that the % mode is selected with a readout of 100.0. The test routine (which has the time duration that is completed in an instant) provides that the device being tested appears on the panel CPU tape speed readout. If the whole test routine is successful, the word PASS appears on the tape speed readout. If a device or its associated circuitry is defective during the routine, testing is halted and the number of the device which failed remains on the tape speed readout.

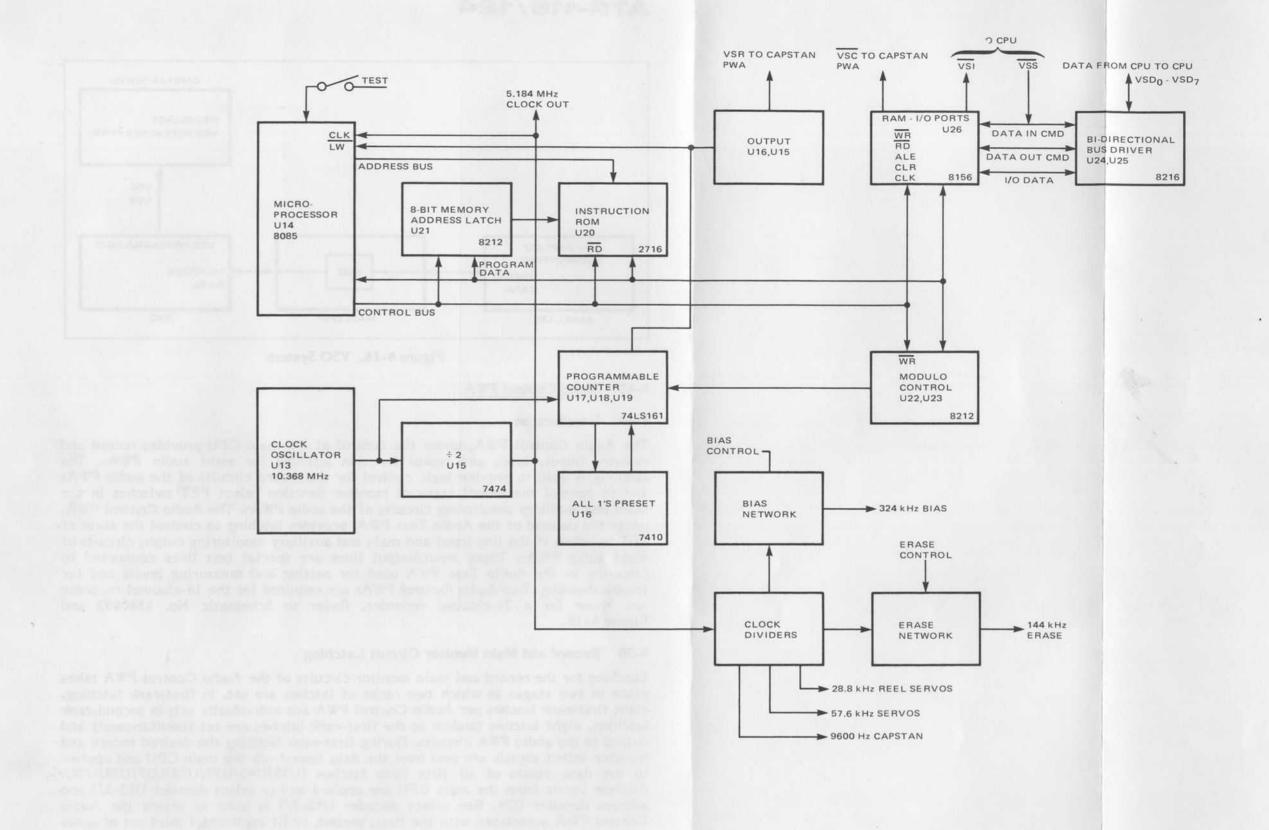


Figure 4-15. VSO Block Diagram

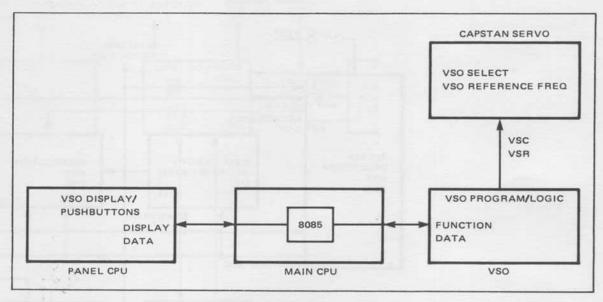


Figure 4-16. VSO System

#### 4-48 Audio Control PWA

#### 4-49 Introduction

The Audio Control PWA, under the control of the main CPU provides record and monitor (input, sync, and repro) function latching for eight audio PWAs. The latching is used to provide logic control for the record circuits of the audio PWAs and to control the on/off state of monitor function select FET switches in the main and auxiliary monitoring circuits of the audio PWAs. The Audio Control PWA, under the control of the Audio Test PWA, provides latching to control the state of FET switches in the line input and main and auxiliary monitoring output circuits of eight audio PWAs. These input/output lines are special test lines connected to circuitry in the Audio Test PWA used for setting and measuring levels and for troubleshooting. Two Audio Control PWAs are required for the 16-channel recorder and three for a 24-channel recorder. Refer to Schematic No. 4840492 and Figure 4-18.

## 4-50 Record and Main Monitor Circuit Latching

Latching for the record and main monitor circuits of the Audio Control PWA takes place in two stages in which two ranks of latches are set. In first-rank latching, eight first-rank latches per Audio Control PWA are individually set; in second-rank latching, eight latches tandem to the first-rank latches are set simultaneously and output to the audio PWA circuits. During first-rank latching the desired record and monitor select signals are sent over the data lines from the main CPU and applied to the data inputs of all first rank latches (U39/U43/U33/U32/U27/U28/U38). Address inputs from the main CPU are applied to bay select decoder U13-2/3 and address decoder U24. Bay select decoder U13-2/3 is used to select the Audio Control PWA associated with the first, second, or (if applicable) third set of audio PWAs. One of its one-of-three select outputs is appropriately jumped to one enabling input of channel decoder U24. Address decoder U24 receives the coded

+ 444

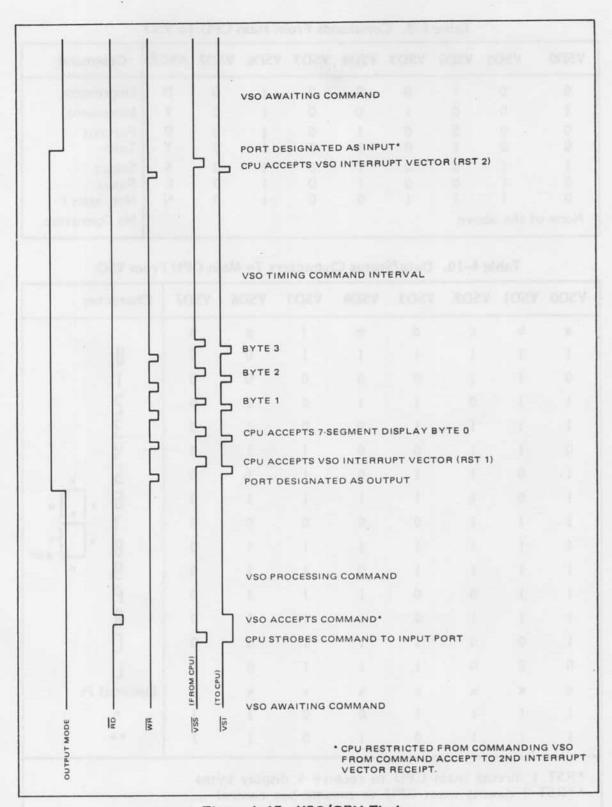


Figure 4-17. VSO/CPU Timing

Table 4-9. Commands From Main CPU To VSO

VSD0	VSD1	VSD2	VSD3	VSD4	VSD5	VSD6	VSD7	ASCII	Command
0	0	1	0	0	0	1	0	D	Decrement
1	0	0	1	0	0	1	0	I	Increment
0	0	0	0	1	0	1	0	P T	Percent Tone
0 0	1 1 1	0 0 1	0 0 1	1 1 0	0	1	0	S R N	Select Reset Non Select
None o	f the ab	ove							No Operation

Table 4-10. Data/Status Characters To Main CPU From VSO

VSD0	VSDI	VSD2	VSD3	VSD4	VSD5	VSD6	VSD7	Character
a	ь	С	d	e	f	g	h	
1	1	1	1	1	1	0	0	0
0	1	1	0	0	0	0	0	
1	1	0	1	1	0	1	0	7
1	1	1	1	0	0	1	0	3
0	1	1	0	0	1	1	0	ų
1	0	1	1	0	1	1	0	5 .
1	0	1	1	1	1	1	0	5 , 16
1	1	1	0	0	0	0	0	]   9
1	1	1	1	1	1	1	0	8
1	1	1	1	0	1	1	0	9 -
1	1	0	0	1	1	1	0	ρ
1	1	1	0	100	1 2	- 1	0	8
1	0	0	1	1	1	0	0	
0	0	0	1	1	1	0	0	
x	x	x	x	х	X	x	1	Decimal Pt
1	1	1	1	0	0	1	1	*
1	1	1	0	1	0	1	1	**

<sup>\*</sup>RST 1 directs main CPU to receive 4 display bytes \*\*RST 2 directs main CPU to resume bus control

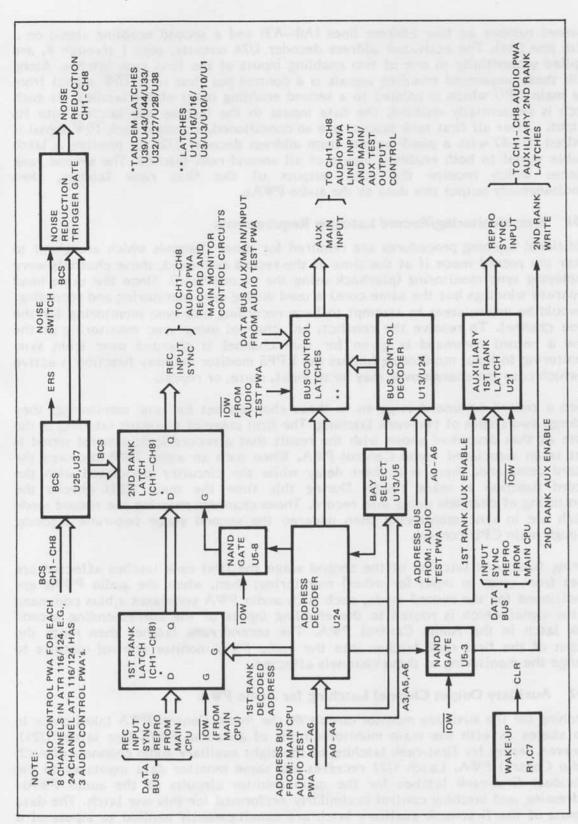


Figure 4-18. Audio Control PWA-Block Diagram

channel number on four address lines (A0-A3) and a second enabling signal on a fifth line (A4). The activated address decoder U24 outputs, pins 1 through 8, are applied sequentially to one of two enabling inputs of the first rank latches. Along with these sequenced enabling signals is a control bus first rank  $\overline{10W}$  signal from the main CPU which is applied to a second enabling input of the latches. As each latch is sequentially enabled, the data inputs to the latches are latched into its output. After all first rank latches are so conditioned, a second rank  $\overline{10W}$  signal is ANDed (U5-8) with a pin-9 output from address decoder U24 to provide a latch enable signal to both enabling inputs of all second rank latches. The second rank latches which receive the data outputs of the first rank latches, then simultaneously output this data to the audio PWAs.

### 4-51 Sync Monitoring/Record Latching Requirements

Additional latching procedures are required for those channels which are about to enter the record mode if at the time of the record command, those channels were employing sync monitoring (playback using the record head). Since the same head (separate windings but the same core) is used during sync monitoring and recording, it would be inconsistent to attempt to have recording and sync monitoring for the same channel. To resolve the conflict, any channel using sync monitoring at the time a record command is given for that channel is changed over from sync monitoring to input monitoring (unless the RPFS monitor memory function is active in which case the change over may be to input, mute, or repro).

When a record command is given to those channels set for sync monitoring, they undergo two stages of two-rank latching. The first stage of two-rank latching is the same as that described above with the result that a record logic control signal is sent to an associated Audio Control PWA. When such an audio PWA receives the record command, there is a short delay while the circuitry associated with the record function is made ready. During this time the main CPU checks the monitoring of channels going into record. Those channels entering the record mode which are in sync monitoring then undergo the second stage two-rank latching through main CPU control.

During first rank latching of the second stage the first rank latches affected are reset from sync to input (or other) monitoring; then, when the audio PWAs are conditioned for the record mode, each such audio PWA generates a bias command status signal which is routed to the enabling inputs of the corresponding second rank latch in the Audio Control PWA. The second rank latches then route the output of the first rank latches into the audio PWA monitor control circuits to change the monitoring of those channels affected.

## 4-52 Auxiliary Output Channel Latching for Audio PWA

Latching for the auxiliary monitor circuit of the Audio Control PWA takes place in two stages as with the main monitor circuit of an audio PWA. One latch (U21), however, serves for first-rank latching of the eight auxiliary audio channels of each Audio Control PWA. Latch U21 receives the same monitor data inputs as do the individual first-rank latches for the main monitor circuits of the audio PWAs. Addressing and latching control is similarly performed for this one latch. The data outputs of the first-rank auxiliary latch are simultaneously applied to inputs of a

second-rank latch located on each of eight associated audio PWAs. The second-rank latching control signal is formed on the Audio Control PWA by the ANDing (U5-3) of a second-rank auxiliary IOW signal and an Audio Control PWA select signal from address decoder U24. This control signal is simultaneously routed to the enabling (clock) input of the second-rank latches on the eight audio PWAs with which it is associated.

When sync monitoring is selected for the auxiliary circuits and this condition is followed by one or more channels entering into the record mode, the state of the auxiliary circuits will change to input monitoring.

#### 4-53 Audio Test Control

For latching operations associated with the Audio Test PWA, refer to paragraph 4-68 on Audio Test PWA operations.

#### 4-54 Electronics Record Status (ERS)

The ERS signal is generated when any channel goes into the record mode. Any channel going into record generates a bias command status (BCS) signal which is applied to NOR gate U9. The output of U9 is routed as the ERS signal to control circuits on the Capstan Servo/Transport Control PWA and is also routed to and processed in the main CPU.

### 4-55 Noise Reduction Trigger (NRT)

The noise reduction trigger circuit provides an open collector logic low to external noise reduction systems via the NRT connector. A +15V level and reference control ground is also provided via the NRT connector. Two modes of operation are available:

- The NRT output for a channel will go low whenever that channel BCS is active.
- The NRT output for a channel will go low whenever that channel has input monitoring selected.

The first mode will always be operational while the second mode will be operational with the NRT INPUT switch on the secondary control panel depressed. The NRT output will then be low in either record, rehearse, or input.

## 4-56 Audio Signal System Functional Description

The main audio consists of up to 16 (24) identical Audio Signal PWAs and four (six) Sync/Repro Preamplifier PWAs. One Audio Signal PWA and its associated preamplifiers comprise the audio signal system for each record/reproduce channel. The audio signal circuits for channels I through 16 (24) are located on PWAs I through 16 (24), respectively, and are located in two (three) bays of the machine, eight cards to each bay (Figure 1-4). An Audio Signal PWA and its associated preamplifier contain the erase, record, reproduce, and audio output circuits for one audio channel. Additionally, circuitry located on the Audio Signal PWA provides bias and erase ramping control, pick-up record capability (PURC), and other timing and control signals required by the audio electronics for that channel. The record and reproduce equalization networks, record and reproduce level presets, bias

normalization preset, and tape-speed and equalization decoding logic are also contained on the Audio Signal PWA. This PWA is capable of being adjusted to provide record and reproduce equalization for four different equalization setups. The secondary control panel equalization switches are used to program equalization switching which occurs with speed selection. Figure 4-19 is a simplified block diagram of the Audio Signal and Preamplifier PWAs for one record/reproduce channel.

The record circuits receive the system audio input and 324-kHz bias, and provide equalization of the receives audio signal to create a recording matching the required equalization at the selected tape speed and/or equalization standard. The record circuits also combine the equalized signal with the 324-kHz bias to provide the drive signal to the record head on the tape transport.

The reproduce circuit receives playback audio from the reproduce head and the Sel-Sync circuit receives playback audio from the record head. These reproduce circuits provide the required playback equalization of each tape signal to match the selected tape speed and/or equalization standard. The selected tape signal is sent to the output amplifier circuits.

The audio output circuits receive the tape and input signals from the reproduce, sync, or input circuits and provide selection and buffering of the tape or input signals to the input/output connectors located in the rear of the machine.

The erase circuit receives a 144-kHz signal which it buffers and amplifies and applies to the erase head via a relay. The reed relay is normally open. Through the record enable and record command signals, the reed relay is energized and the normally open contacts are closed to provide a current path for the erase signal to the erase head. The control signal for the relay is provided via the record tirning logic on the Audio Signal PWA.

The control logic contains PURC circuits which eliminate overlaps and erased gaps in recordings when inserting (dubbing) new material within previously recorded programs. In a recorder system without PURC, initiating the record mode energizes the erase and record heads simultaneously. Since there is a physical distance between the erase head and the record head, a period of over-recording on the unerased tape occurs and, when the dubbing is terminated, an erased gap is left in the program. The length of the over-recording on the tape is determined by the distance between the erase and record heads and the transport tape speed.

The PURC circuits eliminate the over-recording and erase gap by generating a delay between the time that the erase ramping is initiated and the bias/audio ramping is initiated. When the recorder goes into the record mode, the erase ramp-up is initiated first; then, after a delay determined by the selected tape operating speed, the bias/audio ramp-up is initiated. When the recorder is switched out of record mode, the erase ramp-down is initiated first; then after a delay determined by the selected tape operating speed, the bias/audio ramp down is initiated. In this manner, the effect of the physical distance between the erase and record heads is cancelled and the overlap and gap are eliminated from the dubbed portion of the recording.

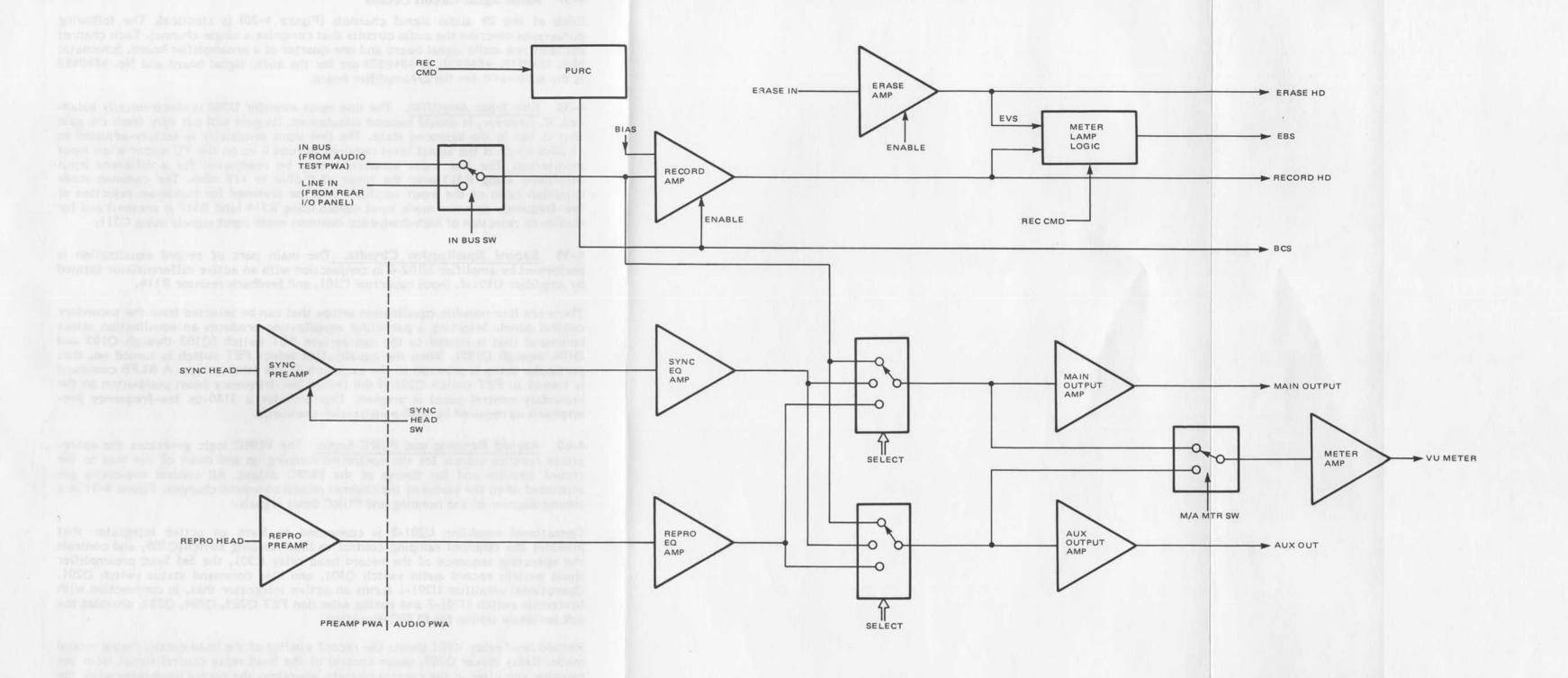


Figure 4-19. Signal System Simplified Block Diagram

### 4-57 Audio Signal Circuit Details

Each of the 24 audio signal channels (Figure 4-20) is identical. The following paragraphs describe the audio circuits that comprise a single channel. Each channel contains one audio signal board and one-quarter of a preamplifier board. Schematic Nos. 4840486, 4840551, or 4840553 are for the audio signal board and No. 4840485 is the schematic for the preamplifier board.

4-58 <u>Line Input Amplifier</u>. The line input amplifer U502 is electronically balanced. If, however, it should become unbalanced, its gain will not vary from the gain that it has in the balanced state. The line input sensitivity is factory-adjusted to +4 dBm which is the signal level required to read 0 vu on the VU meter when input monitoring. The line input sensitivity may be readjusted for a different input sensitivity using R513 over the range of 0 dBm to +12 dBm. The common mode rejection ratio of the input amplifier may be trimmed for maximum rejection of low-frequency common mode input signals using R514 (and R512 if present) and for maximum rejection of high-frequency common mode input signals using C511.

4-59 <u>Record Equalization Circuits.</u> The main part of record equalization is performed by amplifier U102-6 in conjunction with an active differentiator formed by amplifier U101-6, input capacitor C101, and feedback resistor R114.

There are four possible equalization setups that can be selected from the secondary control panel. Selecting a particular equalization produces an equalization select command that is routed to the appropriate FET switch (Q102 through Q105 and Q106 through Q109). When the equalization select FET switch is turned on, that particular setup is selected to the exclusion of the other setups. A RLFB command is routed to FET switch Q101 if the record low-frequency boost pushbutton on the secondary control panel is pressed. This provides a 3180-µs low-frequency preemphasis as required by NAB equalization standards.

4-60 <u>Record Ramping and PURC Logic.</u> The PURC logic generates the appropriate ramping signals for the controlled ramping up and down of the bias to the record circuits and for timing of the PURC delays. All control sequences are intitiated when the status of the channel record command changes. Figure 4-21 is a timing diagram of the ramping and PURC delay signals.

Operational amplifier U201-8 is connected to form an active integrator that provides the required ramping control to bias ramping switch Q309, and controls the operating sequence of the record head relay K301, the Sel Sync preamplifier shunt switch, record audio switch Q301, and bias command status switch Q201. Operational amplifier U201-1 forms an active integrator that, in conjunction with hysteresis switch U201-7 and timing selection FET Q203, Q204, Q205, provides the selcted dealy timing for PURC operation.

Record head relay K301 shunts the record winding of the head except during record mode. Relay driver Q307, under control of the head relay control signal from the ramping amplifier in the control circuits, energizes the record head relay when the channel is not in record mode. When the channel goes to record mode, the head relay control signal goes low and turns off transistor Q307, which deenergizes the

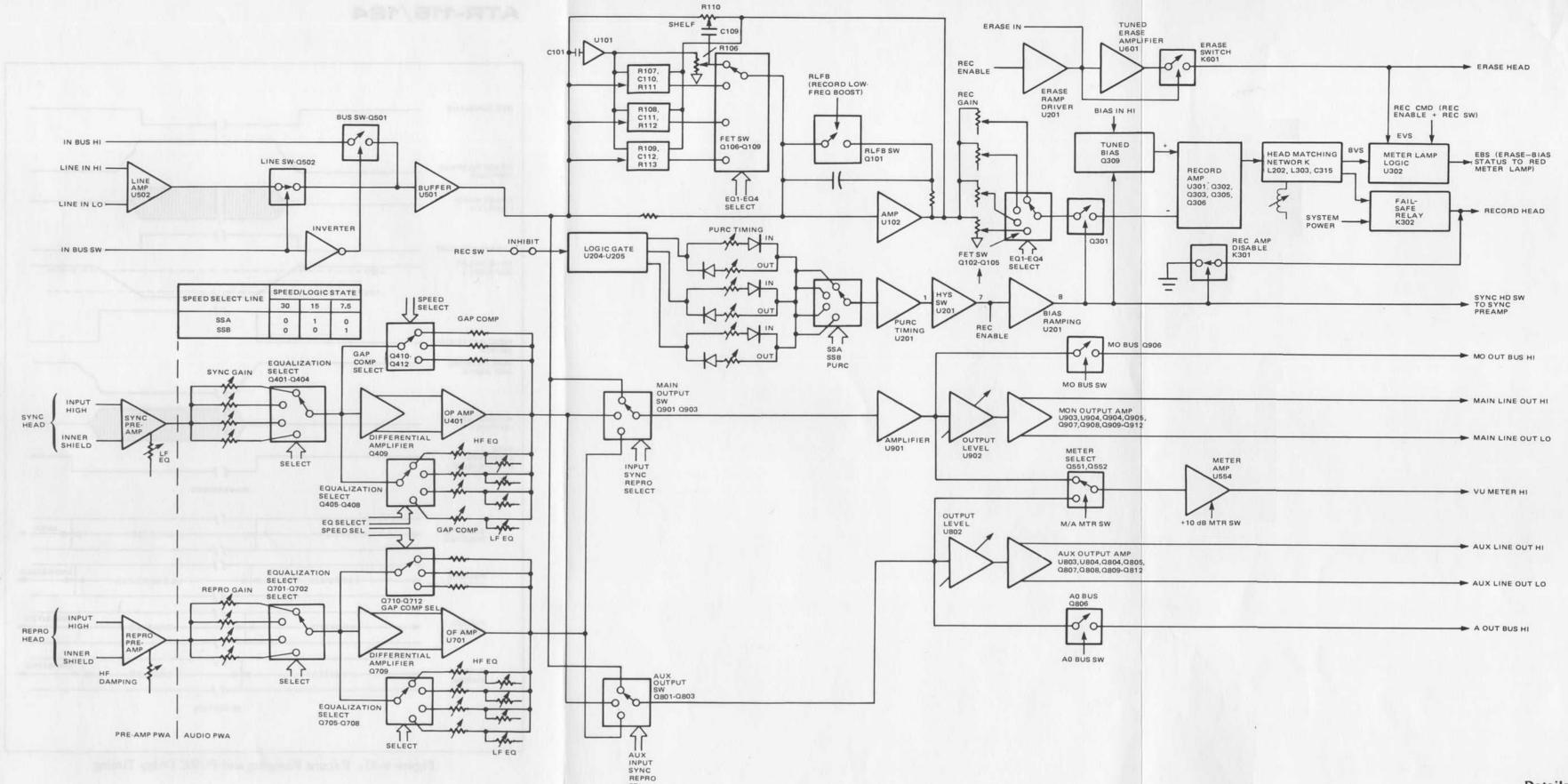


Figure 4-20. Signal System Detailed Block Diagram

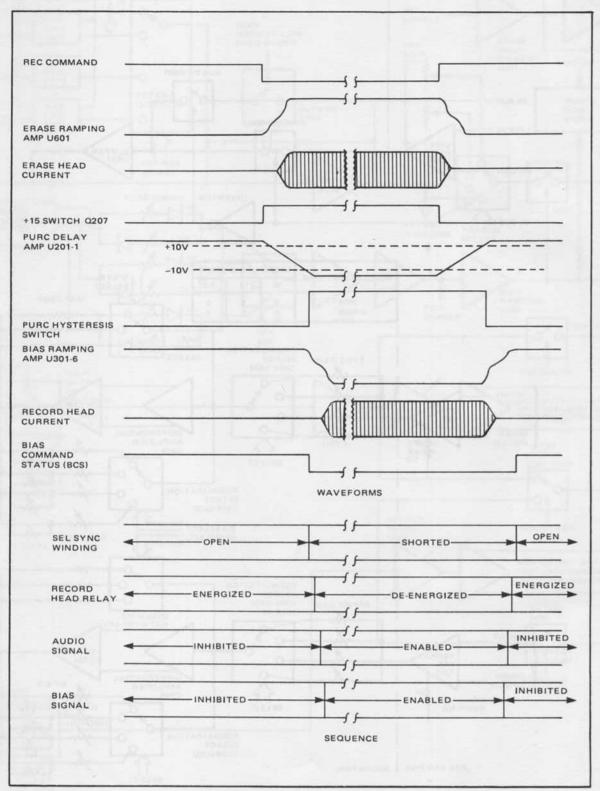


Figure 4-21. Record Ramping and PURC Delay Timing

record head relay. When the relay is deenergized, the contacts across the record winding are opened and the short across the record winding is removed.

Fail-safe relay K302 provides a fail-safe series cutout to the record winding. It is normally energized after system wake-up and will be deenergized on system power failure. Removal of power triggers the power valid signal on the Main CPU PWA.

4-61 Erase Circuit. The erase circuit provides filtering, buffering, and ramping of the 144-kHz erase signal from the master erase bus to the erase head. The erase circuitry receives 144 kHz from the VSO PWA at pin 33/34. The record command controls, via erase ramping control amplifier U601 in the control logic, the rampon and ramp-off of the erase signal to erase amplifier and the erase head.

During record mode, ramping switch Q601 is off and the 144-kHz signal is routed through the erase amplifier to the erase head.

The output of the erase amplifier goes through the contacts of erase relay K601 and then to the erase head. During record, relay K601 is energized by erase head relay driver Q606.

When the channel is not in the record mode, attenuated filtered erase amplifier input is shunted to ground by erase ramping switch Q601, and erase head relay K601 is deeenergized, which opens the circuit to the winding of the erase head. K601 has its coil returned to ground by the power on/off relay in the VSO PWA. This prevents any signal being applied to the erase head during power up or power down.

4-62 <u>Erase Ramping.</u> The turn-on and turn-off of the erase signal is controlled by the record enable and record switch signals from the main CPU. When the channel is not in record mode, the record command is high. The record command is applied to the inverting input of erase ramping amplifier U201. The erase ramping amplifier generates the ramp and control signals for the erase ramping switch (Q601) and the erase head relay driver (Q606).

When the channel is switched into the record mode, the record command goes low. The low record command is applied to the erase ramping amplifier causing the output to start rising to the +12 Vdc level. The erase ramping amplifier together with the ramping network forms an active integrating amplifier that generates an erase ramping signal that is applied to the base of Q601. This signal is used to shape the 144-kHz erase signal at the emitter of Q601. The controlled base drive produces an amplitude-controlled 144-kHz signal which is applied to erase amplifier U601. The erase ramping signal also controls the timing for energizing erase head relay K601 via erase head relay driver Q606.

4-63 <u>Record/Bias Amplification</u>. The 324-kHz bias signal is routed to pin 1 of the Audio Signal PWA from the VSO PWA. Bias level is adjusted by R101 and is applied to record amplifier U301/O302/O303/O305/O306, a bootstrapped supply complementary emitter-follower voltage amplifier.

During record mode, ramping switch Q309 is not conducting and the bias signal is input to the noninverting input of operational amplifier U301. The audio signal to be recorded, after equalization, is routed to the inverting input of U301 via audio switching FET Q301. The bias signal thus produced is then amplified by the record amplifier.

4-64 <u>Erase Bias Status (EBS)</u>. In normal operation, the meter is backlit in red when a channel goes into record. Meter diagnostic circuit U302 indicates lack of erase voltage or record bias voltage by flashing the red meter lamp in a particular sequence. Refer to VU Meter Diagnostics, Table 5-20 in the maintenance section of this manual for further information on this circuit.

The diagnostics are also active if an erase or bias voltage is present when the system is not in record. In this case, the presence of erase or bias at the heads will cause a flashing red indication.

4-65 <u>Reproduce Circuits.</u> The reproduce circuits provide amplification, selection, and post equalization of the playback signals. The reproduce circuit contains the Sel Sync head preamplifier, reproduce head preamplifier, Sel Sync equalizer amplifier, and reproduce equalizer amplifier.

The reproduce head preamplifier receives the playback signal from the reproduce head and is located in the preamplifier bay on the transport. The Sel Sync head preamplifier receives the playback signal from the Sel Sync winding on the record head and is also located in the preamplifier bay on the transport. The outputs of the two head preamplifiers go to the Audio PWA where, via individual gain and equalization controls and an associated equalization amplifier (U401, U701), the signal is applied to monitor selector amplifiers U901 (main) or U801 (auxiliary) where selection among repro, sync, or input is made via FET switches O901-Q903 (main) or Q801-Q803 (auxiliary). The selected output is fed to monitor output amplifier and the auxiliary output amplifier (if selected on those machines so equipped). The line output amplifiers (main and auxiliary) are transformerless, balanced, and differential output line drivers.

4-66 <u>Metering</u>. The metering of the ATR-116/124 signal system consists of three separate circuit functions: meter amplification, meter selection, and meter lamp diagnostics.

Meter selection for main line amplifier or auxiliary amplifier is made when the meter pushbutton is in its depressed or extended position. The switch position determines the level of the meter switch line. This high or low logic signal is routed to transistor switch Q551, Q552 where selection is made.

The meter drive signal, taken from the input of the line out or auxiliary power amplifier, is applied to the inverting input of amplifier U554. The output of this amplifier is routed to the meter. FET switch Q553 can be activated by depressing the +10-dB pushbutton switch on the secondary control panel. Turning this transistor off increases the gain of meter amplifier U554. This feature is useful when using 7.5 in/s alignment tapes (or adjusting bias or response at 7.5 in/s).

4-67 <u>Power-Up Circuit</u>. To prevent excessive line output transients on power up or down, a suppression circuit O913/O914/VR901/VR902/CR13/CR14/CR17/CR18 temporarily clamps outputs to ground.

There are additional power-up circuits in the main and auxiliary monitor output amplifiers and in the VU meter amplifier circuit. The power-up circuit in the meter amplifier circuit prevents pinning the meter needle when the machine is first turned on.

#### 4-68 Audio Test PWA

#### 4-69 Introduction

Through its front panel connectors and controls the Audio Test PWA (Figure 1-3) provides means to access the main input and main and auxiliary output bus testing terminals of all channel audio PWAs of the recorder. This provision eliminates the necessity of making and breaking connections to the individual channel connectors on the rear I/O panel of the recorder, and is particularly useful when making equalization and level adjustments and during signal system troubleshooting. See Schematic No. 4840518 and Figure 4-22.

#### 4-70 Audio Signal Routing

Signal inputs to an Audio PWA channel are connected through the input bus connector (J108) of the panel. With the bus CTL switch S102 set to ON, FET switch O107 and relay K101 in the transmit channel are respectively closed and energized so that a nominal 0-dBm signal at the J108 input will be conditioned to a-5 dBm level at the pin 30 output of the channel. This output is routed on the output bus to the input bus terminals, pin 37/38, of all Audio PWAs (Schematic Nos. 4840493 and 4840486, 4840551, or 4840553). When the channels are under individual control, the state of line input FET switch O501 of a selected channel audio PWA determines whether an input signal is processed in a particular channel.

Signal outputs from a selected audio PWA channel, pin 75 (main) or pin 73 (auxiliary) are routed respectively to the pin 24 main and pin 20 auxiliary output bus terminals of the Audio Test PWA. The state of output FET switches O906 (main) and O806 (auxiliary) in each channel audio PWA determines whether the signals are output respectively from pins 75 and 73. With bus CTL switch S102 of the Audio Test PWA set to on, FET switches O104 and O101 in the respective Audio Test PWA channels will be closed, and a nominal -5-dBm level at pins 24 and 20 will appear at a 0-dBm level at the respective main and aux output connectors of the PWA.

For both signal inputs and outputs, switching control on the channel audio PWAs is directed from the Audio Test PWA through an Audio Control PWA (Schematic No. 4840492), each Audio Control PWA controlling eight channels.

#### 4-71 Switching Control

When a change of channels is required, either the channel increment S104 or decrement S103 switch is pressed. The respective debouncer latch U118-8/11 or

U118-3/6 associated with the pressed switch will then change state and cause display oscillator U131 to operate. Latch and oscillator outputs will then fire one-shot U125 which outputs a timed pulse through NAND gate U113-11 or U113-3 to the respective count-up or count-down input of counter U120 of display counter U114/U120. After the one-shot times out, the count-up or count-down pulse is clocked into counter U120. The incremented/decremented output of U120 is applied to seven-segment decoder U124 which provides the indicated change to DS101, the less significant digit of the two-digit DS101/DS102 LED channel display.

If the selected switch is held down the oscillator will cause the LED display to increment/decrement continuously. Multiple input NAND gate U112 receives the combined output of display counter U114/U120 and provides a master reset to the counters to provide a display that will be sequenced from the highest channel number to the lowest channel number during channel incrementing and vice versa during channel decrementing; i.e., when the counter increments from channel 24 to channel 1 or decrements from channel to channel 24. Jumper J103 is appropriately placed depending on whether 16 or 24 channels are involved.

Each triggered output from one-shot U125 is also applied through NOR gate U129-8 to latch U128-3/11 which outputs a hold signal to the Main CPU PWA indicating to it that the Audio Test PWA requires the use of the common address and data buses. The Main CPU PWA then finishes its current instruction cycle, isolates its data/address lines from the buses, and sends a hold acknowledge signal back to the Audio Test PWA. The hold acknowledge signal enables address and data bus gates U117 and U111 and enables AND gate U129-6 to gate through a 2.592-MHz clock to address counter U115/U116 and channel comparison counter U109/U110. The clock also provides an I/O write clock through data bus gate U111 to the Audio Control PWAs via the data bus.

The fast rate incremented output of address counter U115/U116 is applied through gates U117 and routed via the address bus to the Audio Control PWAs (Schematic No. 48404920). There, the (U24) channel address and (U13) bay select (Channel 1-8, 9-16, or 17-24) decoders provide a latch enable signal to pin 2 of latches U1/U16/U3/U3/U10/U10/U1. These latches receive at their D2, D3, and D4 data inputs, the logic control for the respective auxiliary output bus (pin 100), main output bus (pin 98), and input bus (pin 5) switches on each channel Audio PWA (schematic Nos. 4840486, 4840551, or 4840553).

In addition to the latch enable signal at pin 2, another simultaneous latch enable signal is required at pin 3 of the latches. This is the routed 2.592-Mhz clock which, as already mentioned, is routed through data bus gate U111 on the Audio Test PWA. In summary, the pin 2 enabling input of each latch is enabled in sequence as the address counter of the Audio Test PWA is stepped through a maximum of 24 channels by the 2.592 Mhz clock, whereas the pin 3 enabling input is enabled with each output of the 2.592 Mhz clock. As both inputs in turn are enabled at the same time, the D-input of the latches is latched into the O-outputs.

At a count of 24 clocks, all latches are processed. On the next, or 25th clock, all inputs to NAND gate U122 at the ouput of channel comparison counter U109/U110

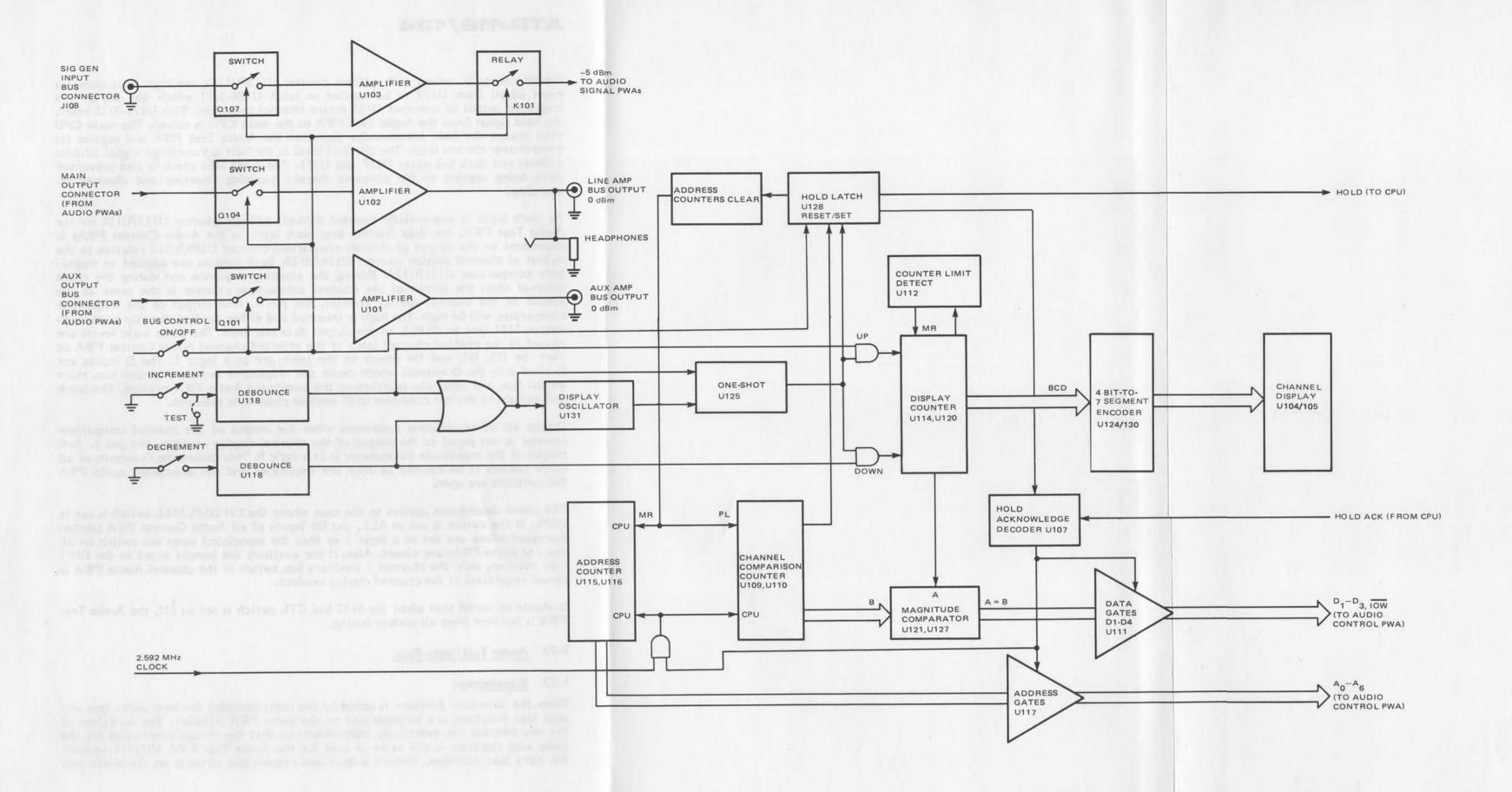


Figure 4-22. Audio Test PWA Block Diagram

(which counts in unison with address counter U115/U116), are high. This causes a reset signal from U122 to be applied to latch U128-3/11 which was set by the triggered output of one-shot U125 during channel selection. With U128-3/11 reset, the hold signal from the Audio Test PWA to the main CPU is raised. The main CPU then lowers the hold acknowledge signal to the Audio Test PWA and regains its control over the bus lines. The changed level in the hold acknowledge signal inhibits address and data bus gates U117 and U111. The 2.592 Mhz clock is also prevented from being applied to the counters thereby stopping counting and channel sequencing.

As each latch is sequentially enabled through address counter U115/U116 on the Audio Test PWA, the data latched into each latch in the Audio Control PWAs is dependent on the output of channel comparison counter U109/U110 relative to the output of channel display counter U114/U120. Both outputs are applied to magnitude comparator U121/U127. During the stepping sequence and during the clock interval when the output of the channel comparison counter is the same as the output of the channel display counter, the pin 6, A=B output of the magnitude comparator will be high. The high is inverted and either applied directly or through switch S101 (set to DSPL), to the output data bus lines. The three logic levels are routed to the enabled channel latch of the selected channel Audio Control PWA so that the D2, D3, and D4 inputs to the latch are at a logic 1. The D inputs are latched into the Q outputs which cause the respective auxiliary output bus, main output bus, and input bus switches on the associated Audio PWA to close. The latch will remain in this set condition until another channel is selected.

During all other stepping sequences when the output of the channel comparison counter is not equal to the output of the channel display counter, the pin 6, A=B output of the magnitude comparator is at a logic 0. This causes the Q outputs of all other latches to be cleared as they are sequenced and the associated audio PWA bus switches are open.

The above description applies to the case where the CH DSPL/ALL switch is set to DSPL. If the switch is set to ALL, the D4 inputs of all Audio Control PWA latches discussed above are set to a logic 1 so that the associated input bus switch on all channel audio PWAs are closed. Also, if the auxiliary bus jumper is set to the CH 1 only position, only the channel 1 auxiliary bus switch in the channel Audio PWA is closed regardless of the channel display readout.

It should be noted that when the S102 bus CTL switch is set to off, the Audio Test PWA is isolated from all system busing.

### 4-72 Audio Test/Auto-Bias

### 4-73 Introduction

When the auto-bias function is opted by the user, circuitry for both audio test and auto bias functions are incorporated on the same PWA 4051011. The functions of the two circuits are essentially independent so that the circuit description for the audio test circuitry is the same as that for the Audio Test PWA 4051010 without the auto bias function. Record output and repro-input circuits on the audio test

circuitry are used by the auto bias circuit during an auto bias operation. Channel selection for signal input and output and the associated channel readout is as described under the audio test circuit description. Interaction between the two circuits is such that the following conditions should be noted.

- When the auto-bias process is in operation, the audio test circuit is disabled.
   Furthermore, audio test operation can be interrupted by initiation of the auto bias process.
- When the auto-bias process is in operation, channel switching may not be accomplished through the audio test increment/decrement circuitry.

### 4-74 Auto Bias Circuitry Description

Refer to block diagram of Figure 4-23 and Schematic No. 4840519. To perform auto-bias for a specific channel, the main setup panel must be set for record operation for that channel and the channel readout of the Audio Test/Auto Bias PWA must be consistent with the setup panel channel selection. When this is accomplished the REPRO switch for the channel is activated, and the PWA READY/SAFE/MANUAL switch is set to READY, the auto bias process may be accomplished through activating of the PWA RUN switch.

When RUN is pressed, a ground signal through the switch causes a logic 1 wake-up line level to be clocked through timing and control flip-flop U214-8/9. The high from pin 9 of the flip-flop causes the following in the audio test circuitry: odisables oscillator/one-shot combination U131/U125 of the channel increment/decrement circuit,

- closes relay K101 of the record input circuitry, and
- · closes FET Q104 in the repro circuit.

In the auto-bias circuitry, the high from pin 9 of U214 activates 40-kHz clock U222-9, causes RUN LED DS 201 to light, and closes audio signal output FET gates Q206 and Q207. The low from pin 8 of U214 triggers one-shot U215 of the timing and control circuit and enables heads distance compensation gates U217/U218. Activated one-shot U215 clocks the high wake-up line level through flip-flop U214-5/6 of the timing and control. The high from pin 5 of U214 provides an enabling input to reset gate U202 at the output of overbias comparator U213. The low from pin 6 of U214 enables 9.9-Hz bias generator clock U222-5.

Under the above conditions, the essential circuits for auto biasing are activated. The 40-kHz output from clock U222-9 is applied to frequency divider U219 which outputs audio frequencies of 20, 10, and 5 kHz. These are associated with respective tape speeds of 30, 15, and 7.5 in/s. Selection of the desired tape speed is made on the secondary control panel via a low SSA (30 in/s), SSB (15 in/s), or SSC (7.5 in/s) logic level signal to a respective FET gate Q205, Q208, or Q209. Attenuators and LC networks at the input to these gates convert the divider square wave outputs to attenuated sinewaves. Heavier attenuation in the 7.5 in/s attenuator results in sinewaves 10-dB lower than those in the 15 and 30 in/s attenuators. The selected frequency associated with its respective tape speed is then routed through output FET gates Q208/Q207 to op amp U103 in the audio test

record channel. The record signal is then routed out on the I-bus to the pin 37 record input of all Audio Signal PWAs.

At the same time that the above occurs, the output of 9.9-Hz oscillator U222-5 is applied to counter U220/U221 through control gates U205. Gates U205 inhibit clocking to the counters in the event 24V power supply should fail. Counter U220/U221 outputs a steady increasing count through heads distance compensator U217 and U218 to digital-to-analog converter U211.

Head distance compensators U217/U218 are adders which take into account the distance between the record and repro heads. Because the repro head output is used as the measure of required bias amplitude (to be described), more bias than that required for the record head is generated; i.e., when the repro head output is such that a certain level of bias is determined, too much bias is, in fact, generated via 9.9-Hz clock U222-9. The particular 9.9-Hz frequency was selected because at 30 in/s, the amount of excess bias due to the distance between the record and repro heads is represented by one clock pulse from U222-9. Consequently at 15 and 7.5, the amount of excess bias is represented by respective counts of 2 and 4 clock pulses, since proportionally more counts are generated at these slower tape speeds. Prior to bias level determination, as determined through the repro head, the excess level is added to the U220/U221 counter outputs by U217. At a tape speed of 7.5 in/s a binary 4 (100) is continuously applied to the B inputs of U217, a binary 2 (010) at 15 in/s, and a binary 1 (001) at 30 in/s.

Digital-to-analog converter U211 receives a steadily increasing count from the counters through head distance compensators U217/U218. As such the analog output will be an increasing ramp function which is applied as a bias amplitude control signal through FET Q204 to the auto bias channel (pin 20) of the VSO PWA. This bias level overrides the manually set levels on this PWA and is routed to the pin 1, bias amplitude control inputs of all the 16 or 24 Audio PWAs. When the correct bias level is determined as sensed by the repro head output, the ramp voltage level is terminated. The B-inputs to adder U217 are suppressed and the bias undergoes a downward shift by the amount of the excess due to record and repro head separation. This level is the determined correct level which is stored in CMOS counters U220/U221 and used for bias amplitude control.

In computing the correct amount of bias, the repro signal from pin 75 of the Audio PWA of the selected channel (originally generated through frequency divider U219 as described above) is routed through op amp U102 of the audio test circuit. In the auto bias circuit, the routed 0-dB signal is attenuated 10 dB through R241 for tape speeds of 15 and 30 in/s. For the tape speed of 7.5 in/s, the signal is routed unattenuated through FET O202. In either situation the repro signal is applied through controlled decay envelope detector U224 which converts the ac signal to a dc level. The dc level is applied through two channels, one a direct route to the inverting input of overbias comparator U213, and the other to the noninverting input of U213 through peak detector C218/U212 and overbias select S201/S202.

The amount of overbias as determined by the setting of S201/S202 (up to 6-3/4 dB) is predetermined by the standards set for the kind of tape used. As the linear ramp bias output from D/A converter U211 increases and is combined with the

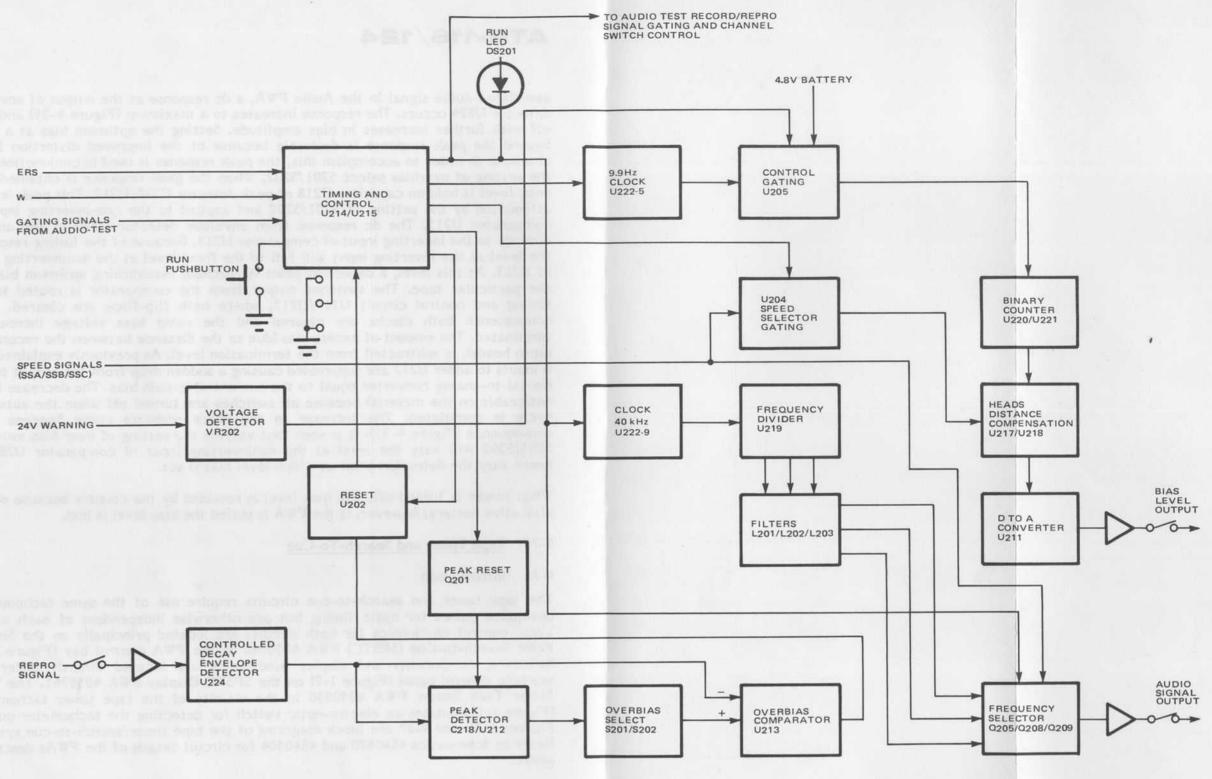


Figure 4-23. Auto Bias Circuit Block Diagram

associated audio signal in the Audio PWA, a dc response at the output of envelope detector U224 occurs. The response increases to a maximum (Figure 4-24) and falls off with further increases in bias amplitude. Setting the optimum bias at a point beyond the peak response is desirable because of the improved distortion levels obtained. In order to accomplish this, the peak response is used in conjunction with the setting of overbias select S201/S202. When the peak response is obtained, this peak level is held on capacitor C218 of peak detector C218/U212. This peak level is attenuated by the setting of \$201/\$202 and applied to the non-inverting input of comparator U213. The dc response from envelope detector U224 is also applied directly to the inverting input of comparator U213. Because of the falling response, the level at the inverting input will fall to the fixed level at the noninverting input of U213. At this level, a detection point is reached, establishing optimum bias for the particular tape. The switched output from the comparator is routed to the timing and control circuit U214/U215, where both flip-flops are cleared. As a consequence both clocks are cleared and the ramp bias voltage increase is terminated. The amount of excess bias (due to the distance between the record and repro heads), is subtracted from the termination level. As previously explained, the B inputs to adder U217 are suppressed causing a sudden drop from the output of the digital-to-analog converter equal to the amount of excess bias. The decrease is not noticeable on the meter(s) because all switches are turned off when the auto-bias cycle is completed. The increase in the repro response curve happens as a consequence (Figure 4-25). It is seen that varying the setting of over bias switches S201/S202 will vary the level at the noninverting input of comparator U2B and hence vary the detection point at which level bias is set.

When power is turned off, the bias level is retained by the counter because of the stay-alive battery; however, if the PWA is pulled the bias level is lost.

### 4-75 Tape Timer and Search-To-Cue

#### 4-76 Introduction

The tape timer and search-to-cue circuits require use of the same tachometer-developed pulses for basic timing but are otherwise independent of each other. Logic control electronics for both circuits are located principally on the Single-Point Search-to-Cue (SPSTC) PWA 4050960 in the PWA control bay (Figure 1-2). Switching components and display electronics are located directly under the machine control panel (Figure 1-2) on the SPSTC Display PWA 4050961. The Tape Timer Tach Sensor PWA 4050950 in the vicinity of the tape timer tachometer (Figure 1-1) contains an electro-optic switch for detecting the tachometer pulses. Figures 4-26 and 4-27 are block diagrams of the tape timer/search-to-cue system. Refer to Schematics 4840480 and 4840504 for circuit details of the PWAs described above.

### 4-77 Tape-Timer Tachometer

The tape-timer tachometer generates timing pulses for both tape-timer and search-to-cue functions. The tachometer is contained on the tape transport assembly (Figure 1-1) and consists of a tape wheel assembly and Tape-Timer Tach Sensor PWA. The tape-driven tape wheel assembly provides one complete rotation for each 7.5 in. of tape motion. The tape wheel assembly contains a shutter which

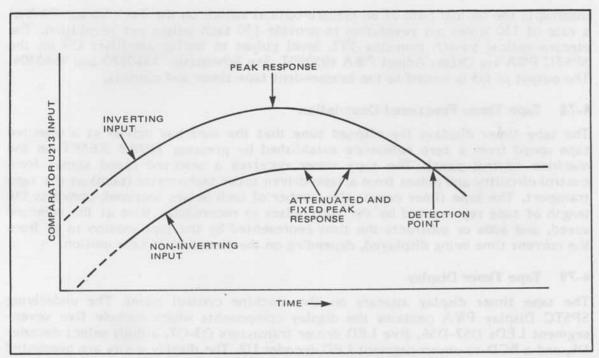


Figure 4-24. DC Repro Signal Response Time

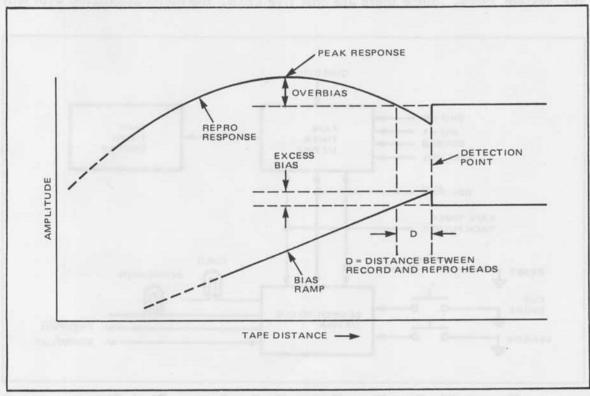


Figure 4-25. Repro Response and Bias Level Inputs Tape Distance

interrupts the optical path of an electro-optical switch on the Tach Sensor PWA at a rate of 150 times per revolution to provide 150 tach pulses per revolution. The electro-optical switch provides TTL level pulses to buffer/amplifier O3 on the SPSTC PWA via Offset Adjust PWA 4050907. See Schematic 4840480 and 4840504. The output of O3 is routed to the independent tape timer and circuits.

### 4-78 Tape Timer Functional Description

The tape timer displays the elapsed time that the tape has moved at a selected tape speed from a zero reference established by pressing TIMER RESET on the machine control panel. The tape timer receives a selected speed signal from control circuitry and pulses from a tape-driven timer tachometer (tach) on the tape transport. The tape timer counts the number of tach pulses received, converts the length of tape represented by the tach pulses to record/play time at the selected speed, and adds or subtracts the time represented by the tape motion to or from the current time being displayed, depending on the direction of tape motion.

### 4-79 Tape Timer Display

The tape timer display appears on the machine control panel. The underlying SPSTC Display PWA contains the display components which include five seven-segment LEDs DS2-DS6, five LED driver transistors O3-Q7, a digit select decoder U4, and a BCD-to-seven-segment LED decoder U2. The display digits are presented on a time multiplexed basis with eight time slots making up a repetitive cycle under control of the 324-kHz system clock with each time slot equal to a period of the system clock. Since there are only five LEDs, the digits associated with only

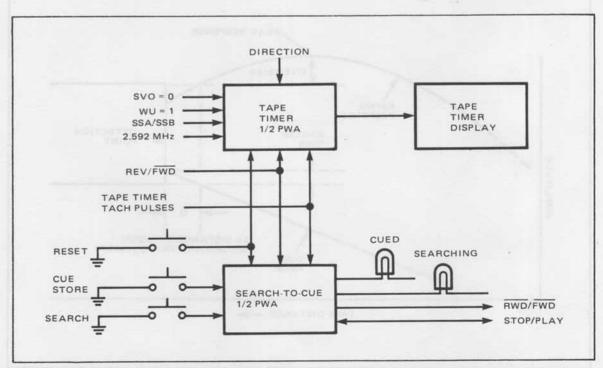


Figure 4-26. Tape Timer/Search-To-Cue-System-Block Diagram

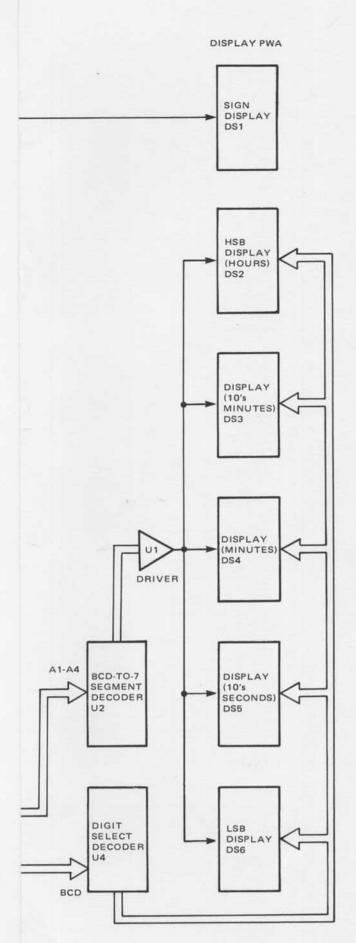


Figure 4-27. Tape Timer Simplified Block Diagram

five time slots can be displayed, the choice of which five depending on the position of jumper J1 of the SPSTC PWA in the control bay. When J1 (Figure 2-7) is in the A-D position, the digits presented are in accord with those on the machine control panel: HOURS, MINUTES, SECONDS (see Table 3-1). For this jumper position the digits associated with time slots t3 through t7 are presented representing units of seconds (t3) through units of hours (t7). When J1 is connected across B-D, there is a downward shift in presentation such that the digits associated with time slots t2 through t6 are displayed, that is, the least significant digit for t2 displaying tenths of a second and the most significant digit for t6 displaying tens of minutes. When J1 is connected across C-D there is a further shift of two time slots, such that the digits associated with time slots t0 through t4 are displayed, that is the most significant digit for t4 displaying tens of seconds and the least significant digit for t0 displaying a divided unit based on the tape speed selected (7.5 in/s, 15 in/s, or 30 in/s). See Figure 4-28 for the digit-time slot relationship.

Each of the processed digits from the counter logic of the timer for each of the eight time slots is routed over four BCD lines to BCD-to-seven-segment decoder U2. The decoded output of U2 provides logic lows to those segments of an LED required to form a number. The lows are simultaneously applied to the cathodes of like segments of all five LEDs, since the cathode elements are in parallel. The anode elements of each LED are connected individually to the respective Q3-Q7 drivers, each driver of which, in turn, is connected to one of the outputs Y3 through Y7 of digit select decoder U4 (Y0, Y1, and Y2 are not connected).

This three-line input to one of eight-line output decoder U4 sequences output lows whose time slots are synchronized to those of the digit inputs to BCD-to-seven-segment LED encoder U2. In this way the proper digit is displayed for each of the five LEDs. As already indicated, selection of which five time slots are used for display is dependent on the way the J1 jumper connection of the SPSTC PWA is connected.

### 4-80 Tape Timer Pulse Conditioning and System Timing

Buffered tach pulses from Q3 of the SPSTC PWA are sent to tach pulse synchronizer U36 that consists of two D-type latches which are clocked by the positive-going edge of a 324-kHz system clock. The tach pulse synchronizer retimes the tach pulses to provide a pulse one 324-kHz clock period wide for each tach pulse received, regardless of the length of the tach pulse.

When a tach pulse is generated, latch U36-10 is set by the positive-going edge of the 324-kHz clock. The output of latch U36-10 goes to latch U36-7 and AND gate U43-1. U36-7 is set to the same state as U36-10 by the positive-going edge of the 324-kHz clock. The output of U36-10 is combined with the output of U36-7 by AND gate U43-1, so that during the interval that U36-10 is first set and the time that U36-7 is set one clock interval later, the output of AND gate U43-1 goes high. During all other conditions, AND gate U43-1 remains low. The pulse output of AND gate U43-1 goes to tach pulse latch U43-3/6. U42-3/6 is an RS-type flip-flop which stores the tach pulse until required by logic of the tape timer.

The system clock for the tape timer is derived from a 2.592-mHz source received from the Main CPU PWA. This clock source is applied to the clock input of clock

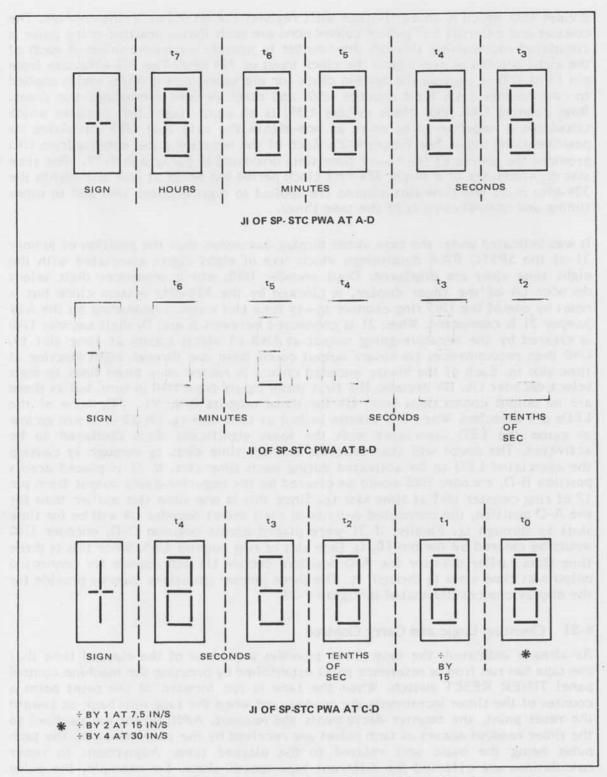


Figure 4-28. Machine Control Panel Elapsed Time Readouts and Associated Cycled Time Slots

divider U39 which is an eight-stage shift register connected as a ring counter. The counter and external U37 gating connections are such that a positive-going pulse is circulated successively through the counter to provide a positive pulse at each of the eight outputs of one-eighth the clock input or 324 kHz. The 324-kHz rate from pin 13 of U39 is used as the system clock for the tape timer circuits and is applied to ring counter U45, digit encoder U40, and other devices throughout the timer. Ring counter U45, like clock divider U39, is an eight-stage shift register which circulates a negative-going pulse at one-eighth the rate that U45 circulates its positive-going pulse. See Figure 4-29. Each of the negative pulse outputs from U45 provides the source of the to--t7 time slots discussed in paragraph 4-79. The time slot durations are of a single 324-kHz clock period but occur at only one-eighth the 324-kHz rate. The time slot outputs are applied to digit encoder U40 and to other timing and control circuits of the tape timer.

It was indicated under the tape timer display discussion that the position of jumper Il of the SPSTC PWA determines which five of eight digits associated with the eight time slots are displayed. Digit encoder U40, which sequences digit select decoder U4 of the timer display, is clocked by the 324-kHz system clock but is reset by one of the U45 ring counter to-t7 time slot outputs depending on the way jumper J1 is connected. When J1 is connected between A and D, digit encoder U40 is cleared by the negative-going output at U45-13 which occurs at time slot t7. U40 then recommences its binary output count from one through eight starting at time slot to. Each of the binary encoded counts is routed over three lines to digit select decoder U4. U4 decodes the first three inputs from U40 in turn, but as there are no output connections from U4 for these outputs (Y0, Y1, Y2), none of the LEDs are affected. When U40 counts to four at time slot t3, U4-12 (Y3) will go low to cause the LED associated with the least significant digit displayed to be activated. The count will then progress through time slots t4 through t7 causing the associated LED to be activated during each time slot. If Jl is placed across position B-D, encoder U40 would be cleared by the negative-going output from pin 12 of ring counter U45 at time slot to. Since this is one time slot earlier than for the A-D position, the connected outputs of digit select decoder U4 will be for time slots to through to. Finally, if JI were placed across position C-D, encoder U40 would be cleared by the pin 10, t4 time slot of ring counter U45. Since this is three time slots earlier than for the A-D position, decode U4 will decode for connected outputs at time slots to through t4. The three jumper situations thereby provide for the display choices illustrated in Figure 4-28.

### 4-81 Counting Logic and Carry Control

As already indicated, the tape timer provides a readout of the elapsed time that the tape has run from a reference point established by pressing the machine control panel TIMER RESET switch. When the tape is run forward of the reset point a counter of the timer increments the readout and when the tape runs back or toward the reset point, the counter decrements the readout. Addition (or subtraction) to the timer readout occurs as tach pulses are received by the timer counter, the tach pulse being the basic unit related to the elapsed time. Adjustment to timer calculations are effected for different tape speeds since, for example, the pulse generation rate is twice as fast at 15 in/s as at 7.5 in/s. Timing calculations are performed cyclically and continuously over eight time periods (t0--t7) of the

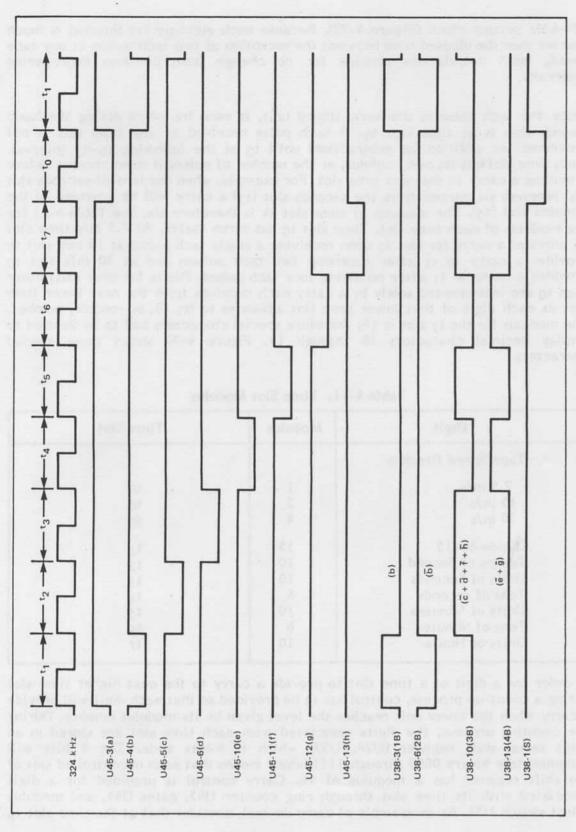


Figure 4-29. Ring Counter U45 Time Slot Generation

324-kHz system clock (Figure 4-29). Because each eight-period interval is much shorter than the elapsed time between the reception of two tach pulses at any tape speed, most calculations provide for no change from previous eight-period intervals.

Since the tach pulse is the basic timing unit, it must be added during the basic period, that is at time slot to. A tach pulse received at any time slot is not processed for addition (or subtraction) until to of the following to-t7 interval. Each time slot has its own modulus, or the number of pulses it must receive before providing a carry to the next time slot. For example, when the tens-of-seconds slot (t4) receives six carries from the seconds slot (t3) a carry will be provided to the minutes slot (t5). The modulus at time slot t4 is therefore six. See Table 4-11 for the modulus of each time slot. Time slot to has three states. At 7.5 in/s time slot to provides a carry for slot to upon receiving a single tach pulse; at 15 in/s slot to provides a carry to to after receiving two tach pulses; and at 30 in/s slot to provides a carry to t<sub>1</sub> after receiving four tach pulses. Digits for time slots other than to are incremented solely by a carry each receives from the next lower time slot as each digit of that lower time slot advances to its 10, or module, number. The modulus for the t<sub>1</sub> slot is 15; therefore special characters had to be devised to display decimal characters 10 through 14. Figure 4-30 shows these special characters.

Table 4-11. Time Slot Modulus

Digit	Modulus	Time Slot	
Tape Speed Divider:			
7.5 in/s	1	t <sub>0</sub>	
15 in/s	2	to	
30 in/s	4	t <sub>0</sub>	
Divide-by-15	15	t <sub>1</sub>	
Tenths of Second	10	t <sub>2</sub>	
Units of Seconds	10	t3	
Tens of seconds	6	t4	
Units of Minutes	10	t5	
Tens of Minutes	6	t <sub>6</sub>	
Units of Hours	10	t7	

In order for a digit of a time slot to provide a carry to the next higher time slot during a count-up process, control has to be provided so that each digit will provide a carry when the lower unit reaches the level given by its modulus number. During the counting process, the digits associated with each time slot are stored in an 8-bit serial shift register (U28, U33) which is 4-bits wide. The 4 bits will accommodate binary 0000 through 1111 which means that each uncontrolled slot of the shift register has a modulus of 16. Carry control is provided for a digit associated with its time slot through ring counter U45, gates U44, and modulus select switch U38. As an example of carry control, consider that at the time slot t6

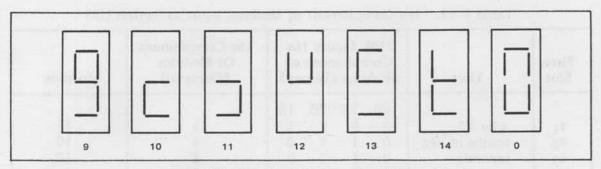


Figure 4-30. Readout Progression (Partial) of Divide-by-15 Digit Display (MOD-15)

(tens of minutes) that a carry is required for time slot t7 (units of hours) when the digit associated with time slot to accumulates to a count of 6 (0110). The carry control therefore adds 10 (1010) or the 16s complement of the modulus for time slot t6 (10000 {10} - 0110 {6} = 1010 {10}) to the accumulated count to provide the carry to the t7 time slot. At time slot t6 pin 12 of ring counter U45 goes low. The gating logic at the output of U45 provides the binary numbers for the particular 16s complement required 1, 0, 1, 0 to the respective 4B, 3B, 2B, 1B inputs of modulus select switch U38. The 16s complement of the modulus for the other digits are similarly provided through ring counter U45 in association with gates connected to the output of U45. Generation of the 16s complement of the modulus for time slots t<sub>1</sub> through t<sub>7</sub> can be graphically determined through Figure 4-29 which includes representation of the B-inputs to modulus select switch U38, a two-state switch. At time slot to, the output from pin 3 (a logic 0) of ring counter U45 switches U38 so that the A-inputs to U38 are accepted by U38. The modulus logic received by the A-inputs are determined by SSA, SSB inputs from the Main CPU PWA. The logic of the SSA and SSB inputs are determined by the selection of the tape speed.

Table 4-12 summarizes the 16s complement for each time slot. The Y outputs of modulus complement switch U38 are routed to the timer counter circuits to test for carry generation during the count-up and count-down modes.

#### 4-82 Initialization

Pressing TIMER RESET routes a ground pulse to the reset inputs of 8-bit serial shift register U28, U33 clearing the register and consequently the timer readout of the machine control panel. The shift register is also cleared when power is initially applied to the machine by the system wakeup signal  $(\overline{WU})$ , which is applied to the reset inputs.

#### 4-83 Count-Up Mode

In the count-up mode, a timer/counter adds up timer tach pulses as they are received to update the timer display. As already indicated, calculations are accomplished on a cyclical basis spread over eight time periods (t0-t7) of the 324 kHz system clock. The timer/counter main components are modulus select switch U38, control gates U27, U32, shift register U28, U33, adder U34, modulus complement adder U29, tach pulse/carry flip-flop U36-2/3, count direction flip-flop U36-14/15, and control gates U31.

Table 4-12. 16s Complement of Modulus Input to Switch U38

Time Slot	Unit	U38 Inputs 16s Complement of Modulus (Binary)			of	16s Complement Of Modulus (Decimal)	Modulus
		4B	3B	2B	1B		
t <sub>1</sub>	÷ by 15	0	0	0	1	1	15
t2	tenths of sec	0	1	1	0	6	10
t3	seconds	0	1	1	0	6	10
t4	tens of sec	1	0	1	0	10	6
t5	minutes	0	1	1	0	6	10
t <sub>6</sub>	tens of min	1	0	1	0	10	6
t7	hours	0	1	1	0	6	10
	all deep not had	4A	3A	2A	1A	So. (0101) 01 1006-1	
t <sub>0</sub>	7.5 in/s (÷ by 1) 15 in/s	1	1	1	1	15	1
	(÷ by 2) 30 in/s	1	1	1	0	14	2
Co. Co.	( ÷ by 4)	1	1	0	0	12	4

During count-up the tape is moving forward of the reset location and a logic low (FWD) true direction signal (TDR) is routed from the Capstan Servo PWA to one input of exclusive-OR gate U23-3. The other input to U23-3 is set to zero by J-K flip-flop U26-11/12 which is preset by the rest signal. The resultant logic 0 from U23-3 is clocked through count direction D flip-flop U36-14/15 to enable AND gate U31-11 and disable AND gate U31-3.

Adder U34 receives the output of both AND gates and the output of shift register U28, U33. Since AND gate U31-3 is disabled, the B inputs to adder U34 are held at a logic 0 in the count up mode. Enabled AND gate U31-11 passes received tach and carry pulses from tach pulse/carry flip-flop U36-2/3 to the carry (C0) input of adder U34. Shift register U28, U33 routes with each clock of the 324-kHz system clock, the contents of its eight to—t7 time slots in succession to the A inputs of U34.

As indicated, the carry input (C0) to U34 receives two inputs:

- Fundamental unit related to time, the tach pulse at time to.
- Carry inputs for digits at the other time slots.

When a tach pulse is received, it is stored in latch U42-3/6 as described in paragraph 4-80. Reception of the pulse can occur at any time but it will not be counted except at time slot to. A received tach pulse is stored until the following to time slot arrives. At to, pin 13 (h) of the ring counter U45 goes low enabling AND gate U42-11 at the output of latch U42-3/6. At to, the tach pulse is routed through U42-11 to the D input of tach pulse/carry flip-flop U36-2/3. On the

following time slot, t<sub>0</sub>, the 324-kHz system clock will clock the pulse through U36-2 to the carry input of adder U34 via enabled gate U31-11. At the same time the 324-kHz system clock will clock shift register U28, U33 so that a four bit binary value of the shift register at time slot t<sub>0</sub> will be applied to the A-inputs of adder U34. The sum of the A and carry inputs to adder U34 is output from its summing terminals to the timer display and to the A-inputs of modulus complement adder U29. Whether the binary encoded digit (at time slot t<sub>0</sub>) to digit decoder U2 of the timer display is displayed is dependent on the way J1 of the SPSTC PWA is connected as described in paragraph 4-79. The A-inputs to modulus complement adder U29 are summed with the modulus complement received by its B inputs from modulus complement switch U38 through AND gates U32. In the count-up mode AND gates U32 are enabled by flip-flop U36-14/15. A carry input (C0) to U29 is held at logic 0 in the count-up mode by AND gate U31-3 which is held disabled by flip-flop U36-15.

The A and B inputs to U29 provide a carry at the C4 output of U29 when the summed inputs equal a binary 16. In paragraph 4-81 there is a description of how a carry was generated in a four-bit binary adder through the addition of a 16s complement of a number to the number itself. It was also indicated that because display calculations are repeated at a rate much faster than the time span between the reception of two tach pulses, most calculations provide for no change in the display from one calculation period to the next. When no tach pulse is received, the summed output from adder U34 will be the same as it A-inputs. Also, the summed A and B inputs to modulus complement adder U29 will then be less than 16, so the (C4) carry output will be logic 0. With C4 at logic 0, the data select inputs to shift register U28, U33 will be low so that the four D0 inputs to U28, U33 will be selected to be routed through the register. As the D0 inputs are connected in parallel to the display lines and the outputs from adder U34, the same binary digits at to will be clocked back into the to slot for the shift register. For time slots to through t7, the individual time slot values from U28, U33 will be clocked into the A inputs of adder U34, but since there has been no increase in the indicated time, the C0 input to U34 will be zero for each time slot and the values will be recirculated back through the D0 inputs of U28, U33 as described for time slot to-

Following timer reset, the arrival of the first tach pulse will result in a binary summed output of 0001 from adder U34 to the A inputs of modulus complement adder U29 at time slot to. At a 7.5 in/s tape speed, the B inputs to U29 would receive a modulus 16s complement of binary 1111 so that a carry from C4 of U29 would be generated immediately. At tape speeds of 15 and 30 in/s, respectively, two and four tach pulses would have to be received before a carry is generated since respective 16s complements of 1110 and 1100 are routed to the B inputs of U29 for those tape speeds during the to time slot.

The first generated carry from C4 will be applied to the D input of tach pulse/carry flip-flop U36-2/3 through gates U43-13 and U42-8. The high from C4 will also be applied to the data select inputs of shift register U28, U33 causing the register to accept data through the four D1 inputs to the register. The D1 inputs to the register receive the outputs of gates U27 which are disabled by count direction flip-flop U36-14/15 in the count-up mode. The next 324-kHz clock following the carry generation will therefore clock a binary 0000 into the to slot for the shift register, thus clearing that time slot.

This same clock pulse following carry generation also clocks the carry through tach pulse/carry flip-flop U36-2/3 to the C0 carry input of adder U34 at time slot t1. The carry is then added to the A inputs of U34 which are now receiving the 4-bit wide contents of shift register U28, U33 for time slot t1. Since this is a binary 0000, a resultant binary sum of 0001 will be sent to timer display digit decoder U2 and to the A inputs of modulus complement adder U29. Since the 16s complement of the modulus at the B inputs of U29 for time slot t1 is 0001 (Table 4-12), no carry will be generated from C4 of U29. The 0001 from adder U34 will therefore be recirculated through the D0 inputs of shift register U28, U33 for the t1 time slot, while a 0000 will be circulated through the remaining time slots. Not until a total of 15 carries are generated from U29 during time slot t1 will a carry be generated for the 10th-of-second time slot at t2. The same process continues for the remaining time slots with the modulus for each time slot determining when a carry will be generated for the next-higher time slot. Figure 4-31 summarizes the preceding description.

#### 4-84 Count-Down Mode

In the count-down mode, the tape moves back toward the reset point with the result that the timer display is decremented. Logic control on the timer is such that as a digit for one time slot is decremented from its modulus value to one less, e.g., 0 to 9 in the minutes position (t5) or 0 to 5 in the tens of minutes position (t6), a borrow is made from the next higher digit position to decrement the value of the higher digit by one, e.g., as in 50 to 49 minutes.

As in the count-up mode, the tach pulse is the basic time-related unit used in decrementing calculations. In reverse of the count-up mode the tach pulse is used in decrementing the fundamental unit in the to time slot position. A borrow rather than a carry is generated to decrement digits in all the higher time slot positions from to through to.

In the count-down mode, the true direction signal from the Capstan Servo PWA is such as to condition count direction flip-flop U36-14/15 so that a tach (or borrow) pulse from tach pulse/carry flip-flop U36-2 is directed to the four B inputs of adder U34 and to the carry in (C0) input of modulus complement adder U29 through AND gate U31-3. AND gate U31-11 at the output of flip-flop U36-14/15 is disabled so that the input to the carry in (C0) input of adder U34 is a constant logic 0 in the count-down mode. The pin 14 output of count direction flip-flop U36-14/15 also disables four AND gates U32 so that the four B inputs to modulus complement adder U29 are a constant logic 0 in the count down mode.

Timing synchronization is the same in the count-down mode as in the count-up mode. A tach pulse received by tach pulse latch U42-3/6 during any to through to calculation period is not counted until time slot to of the following period. At to, as in the count-up mode, pin 13 of ringer counter U45 outputs an enabling pulse to AND gate U42-11 at the output of tach pulse latch U42-3/6. If a tach pulse was received prior to to by latch U42-3/6, it is gated into the D-input of flip-flop U36-2/3. The following 324-kHz system clock pulse at time slot to will then clock the pulse through AND gate U31-3 to the B inputs of adder U34 and the C0 input of modulus complement adder U29. At this point, the B inputs to adder U34, now at a binary 1111, will be added to the binary digits at the A inputs which are received

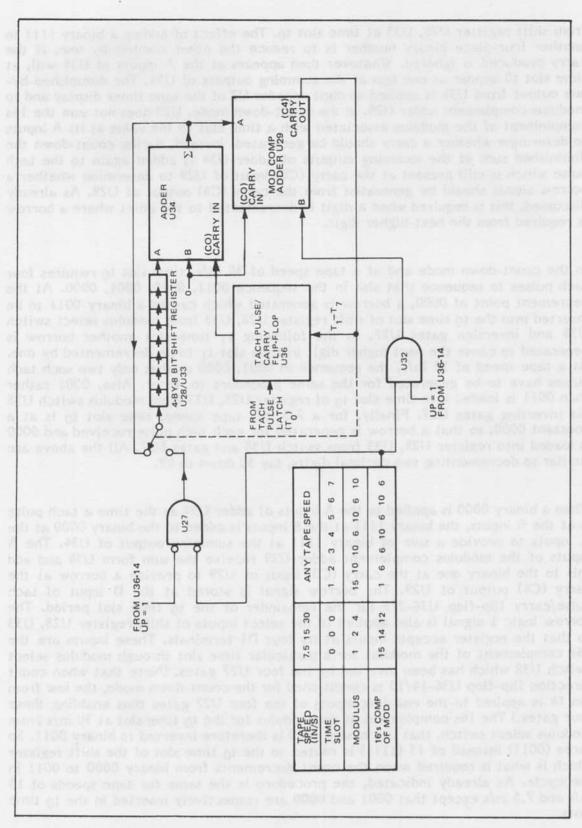


Figure 4-31. Count-Up Logic-Simplified Block Diagram

from shift register U28, U33 at time slot to. The effect of adding a binary 1111 to another four-place binary number is to reduce the other number by one, if the carry produced is ignored. Whatever then appears at the A inputs of U34 will, at time slot to appear as one less at the summing outputs of U34. The diminished-by-one output from U34 is applied to digit decoder U2 of the tape timer display and to modulus complement adder U29. In the count-down mode, U29 does not sum the 16s complement of the modulus associated with a time slot to the value at its A inputs to determine whether a carry should be generated. Instead, during count-down the diminished sum at the summing outputs of adder U34 is added again to the tach pulse which is still present at the carry (C0) input of U29 to determine whether a borrow signal should be generated from the carry (C4) output of U29. As already discussed, this is required when a digit is decremented to the point where a borrow is required from the next-higher digit.

In the count-down mode and at a tape speed of 30 in/s, time slot to requires four tach pulses to sequence that slot in the sequence 0011, 0010, 0001, 0000. At the decrement point of 0000, a borrow is generated which causes a binary 0011 to be inserted into the to time slot of shift register U28, U33 from modulus select switch U38 and inversion gates U27. In the following to time slot another borrow is generated to cause the next higher digit in time slot to be decremented by one. At a tape speed of 15 in/s, the sequence in 0001, 0000 so that only two such tach pulses have to be generated for the same procedure to occur. Also, 0001 rather than 0011 is loaded into time slot to of register U28, U33 from modulus switch U38 via inverting gates U27. Finally, for a 7.5 in/s tape speed, time slot to is at a constant 0000, so that a borrow is generated for each tach pulse received and 0000 is loaded into register U28, U33 from switch U38 and gates U27. All the above are similar to decrementing two decimal digits, say 50 down to 49.

When a binary 0000 is applied to the A inputs of adder U34 at the time a tach pulse is at the B inputs, the binary 1111 at the B inputs is added to the binary 0000 at the A inputs to provide a sum of binary 1111 at the summing output of U34. The A inputs of the modulus complement adder U29 receive the sum form U34 and add this to the binary one at the carry (CO) input of U29 to provide a borrow at the carry (C4) output of U29. The borrow signal is stored at the D input of tach pulse/carry flip-flop U36-2/3 for the remainder of the to time slot period. The borrow logic 1 signal is also applied to the select inputs of shift register U28, U33 so that the register accepts inputs at its four D1 terminals. These inputs are the 16s complement of the modulus for a particular time slot through modulus select switch U38 which has been inverted by the four U27 gates. (Note that when count direction flip-flop U36-14/15 is conditioned for the count-down mode, the low from pin 14 is applied to the enabling inputs of the four U27 gates thus enabling these four gates.) The 16s complement of the modulus for the to time slot at 30 in/s from modulus select switch, that is a binary 1100 is therefore inverted to binary 0011. So three (0011) instead of 15 (1111) is routed to the to time slot of the shift register which is what is required when the count decrements from binary 0000 to 0011 in the cycle. As already indicated, the procedure is the same for tape speeds of 15 in/s and 7.5 in/s except that 0001 and 0000 are respectively inserted in the to time slots.

A borrow signal applied to the D-input of tach pulse/carry flip-flop U36-2/3 during the to time slot as described above, is clocked through the flip-flop to adder U34 and modulus complement adder U29 to decrement a digit in the to slot of the shifts register in the same way as described for the to slot. As other borrows are generated, the process continues for to through to a required. In the simplest and most usual case, no tach pulse is received for a calculation cycle and the same digits are recycled as in the count-up mode. Figure 4-32 summarizes the preceding description.

#### 4-85 Search-To-Cue

A cue point may be established by pressing CUE STORE on the machine control panel. Regardless of whether the machine is playing in a forward or reverse direction, pressing the CUE STORE switch causes a counter to count up in either direction from the cue point. A subsequent pressing of the machine control panel SEARCH switch causes the tape to rewind toward the cue point in a fast mode. As the tape rewinds, the counter counts down to zero. Near the zero count, the counter is caused to decelerate, and at the count of zero, the cue point is identified and a stop command is generated to halt the tape.

The search-to-cue circuit components are indicated on Schematic No. 4840504 and Figure 4-33. When the tape is playing in the forward direction and CUE STORE is pressed, a reset signal is applied to the load inputs of a counter consisting of cascaded binary up/down counters U2, U7, U12, U17, U22, and U51, thereby clearing them. The reset signal is also applied to the clearing input of sign flip-flop U11-9. The resulting logic zero from pin 9 of U11 is applied to pin 5 of exclusive OR gate U23-6. Pin 4 input to U23-6 receives the pin 5 output of direction sense flip-flop U19-5/6. In forward play, a logic zero direction signal from the Capstan Servo PWA is received at pin 74 and clocked through U19-5/6 to pin 4 of gate U23-6. The resulting logic 0 output from U23-6 is applied to the direction (D/U) inputs of the binary counters so that the counter up-counts when receiving tach pulses from the tape timer tachometer through pin 73. Each tach pulse is equivalent to 0.05 in. of tape travel. The counter outputs progress from 20 at pin 3 of binary counter U2 to 223 at pin 7 of binary counter U51, the total capacity of the cascaded counters being 224 or 16,777,220 counts (69,905 ft).

When SEARCH is pressed, the tape winds back to the cue point. The logic low from the switch is routed through gates U48-11, U48-8\*, U9-11, and U9-6 to the reset input of search flip-flop U4-9 causing U4-9 to be reset. The resulting logic

\*Search disable flip-flop U4-4 at the input of AND gate U48-8 was set previously either with the warmup signal or, as needed, shortly after counting up from the cue point. In the first instance, the logic-low warmup signal to the pin 3, S input of U4-4 would set pin 4 to a logic one. In the second instance, just following count-up from the cue point, a logic-high would be generated from binary counter U7-7 at a count of 2<sup>7</sup> or 128 tach pulses. This high, equivalent to tape travel of 128 x 0.05 or 6.4 in. of tape, would be routed through NOR gate U13-1 to pin 1 (number 4 priority input) of priority encoder U16 as a low. The resulting low (binary 4) from pin 6 of U16 would be applied to the pin 2, S input of U4-4 to set pin 4 of U4 to a high.

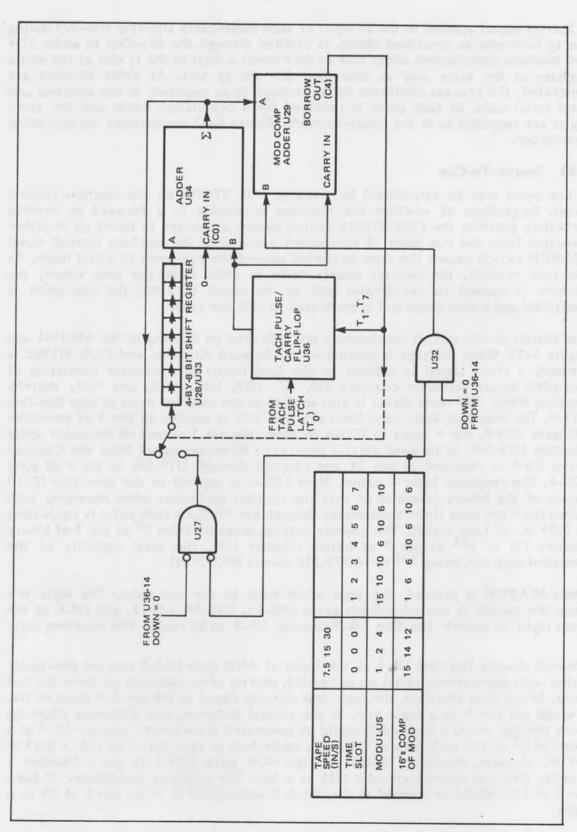


Figure 4-32. Count-Down Logic-Simplified Block Diagram

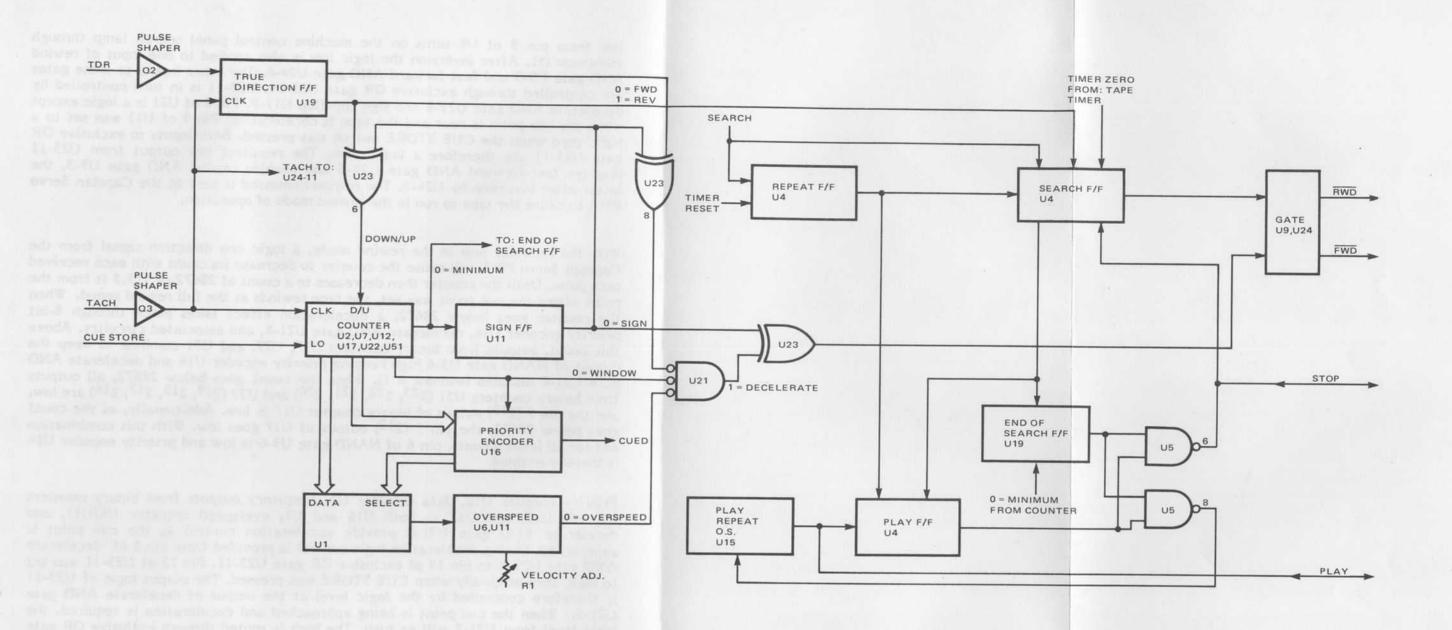


Figure 4-33. Search-To-Cue Simplified Block Diagram

low from pin 9 of U4 turns on the machine control panel search lamp through transistor Q1. After inversion the logic low is also applied to one input of rewind AND gate U9-3 and fast forward AND gate U24-6. The other inputs to these gates are controlled through exclusive OR gate U23-11. U23-11 is in turn controlled by decelerate AND gate U21-8 and sign flip-flop U11-9. Pin 8 of U21 is a logic except when the cue point is near and the tape is decelerating. Pin 9 of U11 was set to a logic zero when the CUE STORE switch was pressed. Both inputs to exclusive OR gate U23-11 are therefore a logic zero. The resulting low output from U23-11 disables fast forward AND gate U24-6 and enables rewind AND gate U9-3, the latter after inversion by U24-3. The rewind command is sent to the Capstan Servo PWA to cause the tape to run in the rewind mode of operation.

With the recorder now in the rewind mode, a logic one direction signal from the Capstan Servo PWA will cause the counter to decrease its count with each received tach pulse. Until the counter then decreases to a count of 28672 or 119.5 ft from the point where the cue point was set, the tape rewinds at the full rewind speed. When the counter goes below 28672, a deceleration effect takes place through 8-bit priority encoder U16, decelerate AND gate U21-8, and associated circuitry. Above this count, outputs from binary counters U17, U22, and U51 combine to keep the output of NAND gate U3-6 high keeping priority encoder U16 and decelerate AND gate U21-8 disabled (window = 1). When the count goes below 28672, all outputs from binary counters U51 (2<sup>23</sup>, 2<sup>22</sup>, 2<sup>21</sup>, 2<sup>20</sup>) and U22 (2<sup>19</sup>, 2<sup>18</sup>, 2<sup>17</sup>, 2<sup>16</sup>) are low, and the pin 7 (2<sup>15</sup>) output of binary counter U17 is low. Additionally, as the count goes below 28672, the pin 3 (2<sup>12</sup>) output of U17 goes low. With this combination and for all lesser counts, pin 6 of NAND gate U3-6 is low and priority encoder U16 is thereby enabled.

Priority encoder U16, data selector U1, frequency outputs from binary counters U2, U7, U12, and U17 to both U16 and U1, overspeed detector U6/U11, and decelerate AND gate U21-8 provide acceleration control as the cue point is approached. During deceleration logic control is provided from pin 8 of decelerate AND gate U21-8 to pin 13 of exclusive OR gate U23-11. Pin 12 of U23-11 was set to logic zero originally when CUE STORE was pressed. The output logic of U23-11 is therefore controlled by the logic level at the output of decelerate AND gate U21-8. When the cue point is being approached and deceleration is required, the logic level from U21-8 will go high. The high is routed through exclusive OR gate U23-11 such that fast forward control AND gate U24-6 is enabled and rewind AND gate U9-3 disabled. Fast-forward control to the Capstan Servo PWA diminishes the tape speed in the rewind direction toward the cue point. When deceleration control is not in effect during rewind, the logic level from U21-8 is low so that rewind gate U9-3 is kept enabled. Control over gates U9-3 and U24-6 is such that the cue point is arrived at without overshoot.

In operation, acceleration control from initial to final stages varies as the cue point is approached. Initially, acceleration control is such that logic highs from pins 3, 2, and 6 of binary counter U17 are routed through NOR gate U13-10 as a logic zero to the pin 4, highest priority (7) input of priority encoder U16. The resulting inverted 7 (binary 000) on the A0, A1, A2 outputs of U16 are routed to the select

inputs of data selector U1. The three logic zeros to U1 cause U1 to select its pin 4 (D0) input so that the level there is routed to its pin 5 output. As a result the frequency output from the pin 3  $(2^4)$  output of binary counter U7 is routed through U1 to overspeed detector U6/U11.

Overspeed detector U6/U11 operates to provide acceleration control whenever two successive pulses to its input are spaced within 4.5 ms of each other (6.5 ms for tape reels larger than 10.5 in. in diameter). The first pulse clocks flip-flop U11-5/6 (whose output at pin 6 is already high). During the clocking interval, the output from pin 8 of 4.5 ms one-shot U6 at the input of U11 is still low, so another high is clocked into the pin 6 output of U11 and nothing is changed. Also, the output of one-shot U6-8 goes high for 4.5 ms after its propagation delay. If a second pulse to U6/U11 follows within the 4.5-ms interval, a low is clocked into the pin 6 output of U11. The resulting low is routed to decelerate NAND gate U21-8 and gates at the output from U21-8 to provide deceleration control to the Capstan Servo PWA as previously described.

As the countdown continues, the outputs from binary counter U17 will all eventually go low and control over priority encoder U16 will be transferred successively to binary counters U12 and then U7. In the process lower priority control outputs from U16 will cause data selector U1 to select higher inputs: D1, then D2, D3, and D4. This will cause the selected controlling frequencies to overspeed detector U6/U11 to increase in turn.

When all counters are cleared upon arrival at the cue point, a minimum signal will be generated by minimum NAND gate U8-8. This minimum signal is used to clock end-of-search flip-flop U19-8/9. If PLAY was not pressed after SEARCH was pressed, a resulting logic 1 from U19-9 is inverted by NAND gate U5-6 and a stop command is sent to the Capstan Servo PWA via pin 53. If PLAY was pressed after pressing SEARCH, a low logic play signal received at pin 57 was routed to play flip-flop U4-13 to reset U4-13. The resulting logic 0 from pin 13 of U4-13 then disabled stop NAND gate U5-8 and enabled play NAND gate U5-8. When the cue point is reached, the other input to U5-8, received from end-of-search flip-flop U19-8/9, goes high. The resulting low from U5-8 then triggers play repeat one-shot U15-6 which generates a play command to the Capstan Servo PWA through pin 57.

Looping or repetitive replaying of a segment of tape can be performed if desired. When CUE STORE has been pressed and tape has played a given amount of time, the length of tape played as indicated by the timer can be replayed on a looping basis by holding down SEARCH and then simultaneously pressing TIMER RESET. This will reset the tape timer to zero and cause the recorder to enter the search mode as preciously described. When the cue point is reached a negative indication of the amount of tape time spent is indicated by the tape time. An end-of-search signal will be generated and the tape will travel at play speed until time tape timer indicates zero. A timer-is-zero signal will then be generated through AND gate U10-4, U9-8, U9-11, and U9-6 to reset search flip-flop U4-9 and the cycle will be repeated (until STOP is pressed).

### 4-86 Power Supply

#### 4-87 Introduction

This section provides a description of the ATR-116/124 power supply. The ATR-116/124 power supply provides the following dc voltage outputs: +5V,  $\pm8V$ ,  $\pm15V$ ,  $\pm25V$ ,  $\pm26V$ ,  $\pm30V$ , and a variable lamp supply. See Table 4—13 for a description of the voltage outputs and their function.

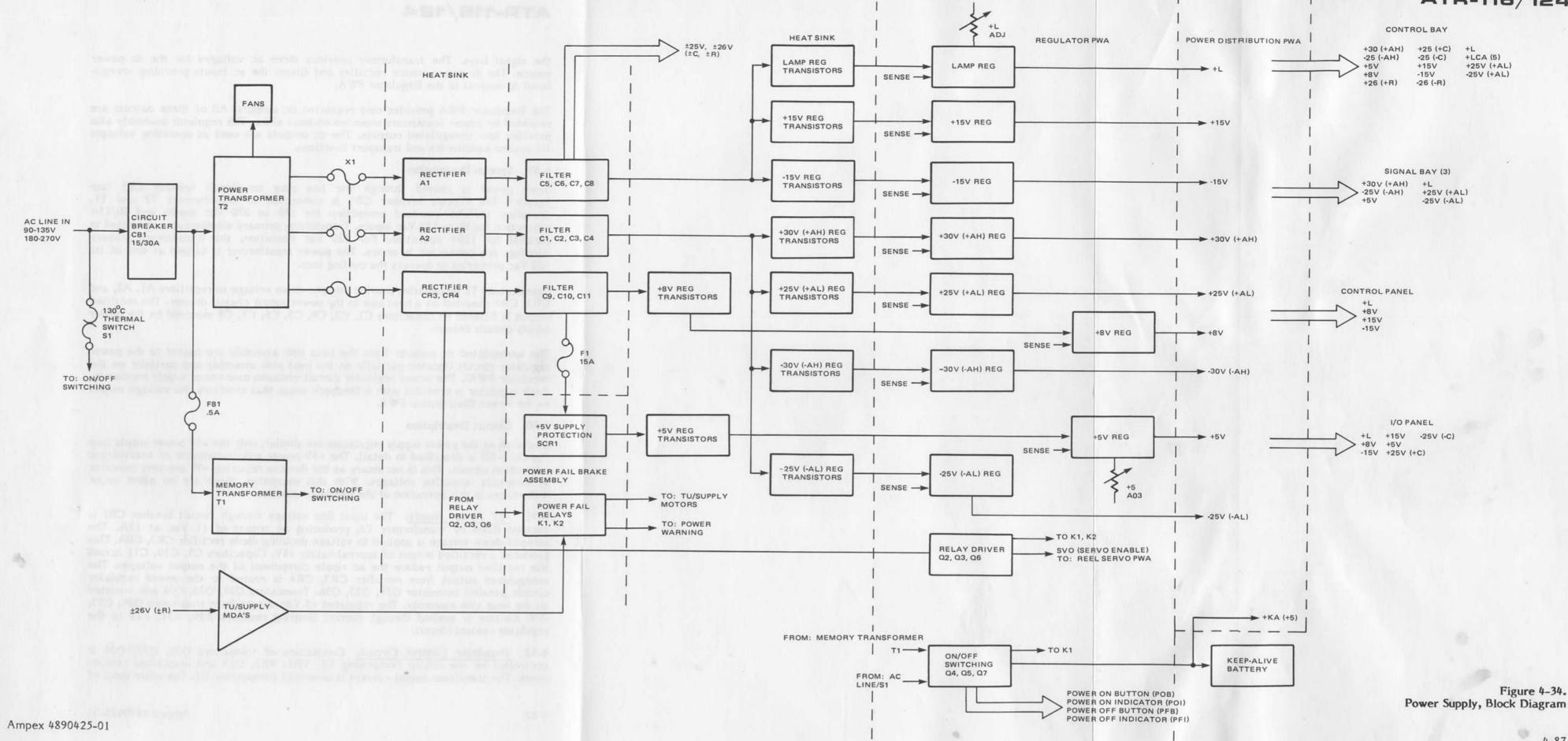
Table 4-13. Power Supplies-Output and Function

Output Voltage	Function				
+5V	Provides regulated +5V for system electronics.				
+L	Provides operator varied regulated voltage source for system indicator lamps.				
+15V	Provides regulated +15V for system electronics.				
-15V	Provides regulated -15V for system electron				
+30V(+AH)	Provides ac regulated +30V nominal for signal system/control system electronics.				
-30V(-AH)	Provides ac regulated -30V nominal for signal system/control system electronics.				
+25V(+AL)	Provides ac regulated +25V nominal for signal system/control system electronics.				
-25V(-AL)	Provides ac regulated -25 nominal for signal system/control system electronics.				
+8V	Provides ac regulated +8V for I/O panel, contr panel, control system electronics.				
±25V(±C)	Provides unregulated ±25V for capstan MDA, lift solenoid, and control system electronics.				
±26V(±R)	Provides unregulated ±26V for takeup and supply MDAs, and control system electronics.				

#### 4-88 Power Supply Functional Description

The power supply (see Figure 4-34) consists of the power chassis assembly, the power transformer, the memory supply transformer and the Power Regulator PWA (see Schematic No. 4840499). The power transistors for the regulator are mounted externally to the regulator on heat sinks. The entire power supply is mounted on the ATR-116/124 chassis on the lower right-hand side, and is contained (with the exception of the power and memory transformers) in a pull-out drawer.

Main power (120 or 240 Vac) is applied through a circuit breaker to the power transformer T2. The circuit breaker is located on the rear of the chassis and is operated by a rod that terminates at the front of the ATR-116/124 to the right of



the signal bays. The transformer provides three ac voltages for the dc power source. The dc power source rectifies and filters the ac inputs providing unregulated dc outputs to the Regulator PWA.

The Regulator PWA provides nine regulated dc outputs. All of these outputs are provided by power transistors mounted on heat sinks. The regulator assembly also provides four unregulated outputs. The dc outputs are used as operating voltages for system electronics and transport functions.

#### 4-89 System Description

Input power is routed through the line plug to circuit breaker CB1 (see Figure 4-34). Circuit breaker CB1 is connected to transformers T2 and T1, providing 15/7.5A overload protection for 180 to 270 Vac inputs and 30/15A protection for 90 to 135 Vac inputs. Transformer primary windings are connected in parallel for 120V operation. For 220 Vac operation, the transformer primary windings are connected in series. The power transformer is tapped at one of its 120 Vac primaries to operate the cooling fans.

Transformer T2 secondaries provide stepped-down voltage to rectifiers A1, A2, and CR3, CR4 mounted on a heat sink in the power supply chassis drawer. The rectified output is filtered by capacitors C1, C2, C4, C5, C6, C7, C8 mounted on the power supply chassis drawer.

The unregulated dc outputs from the heat sink assembly are routed to the power regulator circuit (located partially on the heat sink assembly and partially on the regulator PWA). The power regulator circuit contains nine power supply regulators. Each regulator is provided with a feedback sense that monitors the voltage output to the Power Distribution PWA.

### 4-90 Circuit Description

Inasmuch as the power supply regulators are similar, only the +5V power supply (see Figure 4-35) is described in detail. The +5V power supply contains an overvoltage protection circuit. This is necessary as the devices requiring +5V are very sensitive to incorrect operating voltages. With this exception, there are no other major differences in this operation of the regulator circuits.

- 4-91 +5V Power Supply. The input line voltage through circuit breaker CB1 is stepped down by transformer T2, producing an output of 11 Vac at 12A. The stepped-down voltage is applied to voltage doubling diode rectifier CR3, CR4. This produces a rectified output of approximately +8V. Capacitors C9, C10, C11 across the rectifier output reduce the ac ripple component of the output voltages. The unregulated output from rectifier CR3, CR4 is routed to the power regulator circuit parallel transistor Q34, Q35, Q36. Transistors Q34, Q35, Q36 are mounted on the heat sink assembly. The regulated +5 Vdc output from transistors Q34, Q35, Q36 emitter is applied through current limiting resistors R10, R11, R12 to the regulator control circuit.
- 4-92 Regulator Control Circuit. Conduction of transistors Q34, Q35, Q36 is controlled by the circuit comprising U1, VR1, VR2, Q13 and associated components. The transistor output current is sensed by comparator U1. The other input of

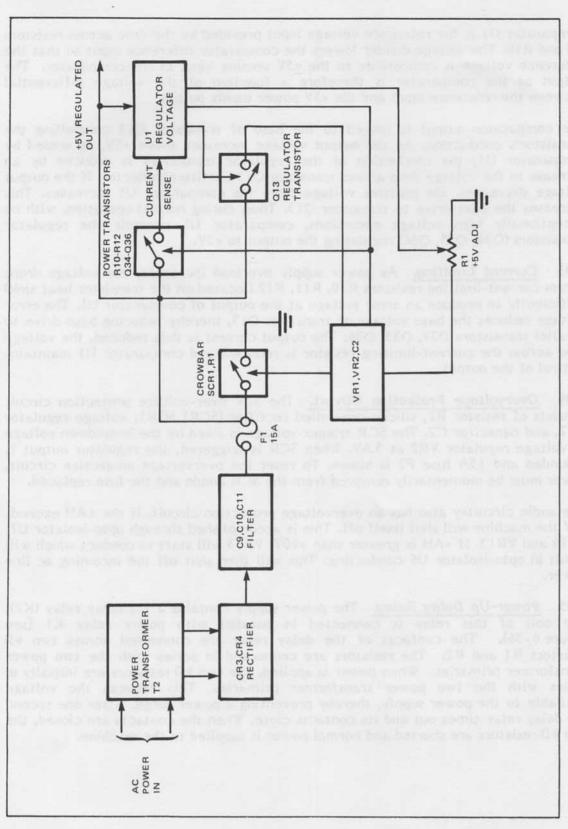


Figure 4-35, +5V Regulator

comparator U1 is the reference voltage input provided by the drop across resistors R8 and R10. The voltage divider lowers the comparator reference input so that the reference voltage is comparable to the  $\pm 5V$  sensing input of the comparator. The output of the comparator is therefore a function of the voltage differential between the reference input and the  $\pm 5V$  power supply output.

The comparator output is routed to the base of transistor Q13 controlling the transistor's conduction. As the output voltage increases above +5V, as sensed by comparator U1, the conduction of the regulator transistors is reduced by an increase in the voltage drop across transistor Q13's emitter/collector. If the output voltage decreases, the positive voltage from the comparator U1 increases. This increases the base drive to transistor Q13. Thus, during normal operation, with no exceptionally high voltage excursions, comparator U1 controls the regulator transistors (Q34, Q35, Q36) regulating the output to +5V.

- 4-93 <u>Current Limiting.</u> As power supply overload increases, the voltage drops across current-limiting resistors R10, R11, R12 (located on the transistor heat sink) sufficiently to produce an error voltage at the output of comparator U1. The error voltage reduces the base voltage of transistor Q13, thereby reducing base drive to parallel transistors Q34, Q35, Q36. The output current is thus reduced, the voltage drop across the current-limiting resistor is reduced, and comparator U1 maintains control of the output.
- 4-94 Overvoltage Protection Circuit. The +5V over-voltage protection circuit consists of resistor R1, silicon-controlled rectifier (SCR) SCR1, voltage regulator VR2, and capacitor C2. The SCR trigger voltage is fixed by the breakdown voltage of voltage regulator VR2 at 5.6V. When SCR is triggered, the regulator output is grounded and 15A fuse F2 is blown. To reset the overvoltage protection circuit, power must be momentarily removed from the SCR anode and the fuse replaced.

The audio circuitry also has an overvoltage protection circuit. If the ±AH exceeds 40V the machine will shut itself off. This is accomplished through opto-isolator U7, VR14 and VR13. If +AH is greater than +40V, VR13 will start to conduct which will result in opto-isolator U6 conducting. This will then shut off the incoming ac line power.

4-95 <u>Power-Up Delay Relay.</u> The power supply contains a 1-s delay relay (K2). The coil of this relay is connected in parallel with power relay K1 (see Figure 4-36). The contacts of the delay relay are connected across two  $4\Omega$  resistors R1 and R2. The resistors are connected in series with the two power transformer primaries. When power is applied, the two  $4\Omega$  resistors are initially in series with the two power transformer primaries. This reduces the voltage available to the power supply, thereby preventing a power surge. After one second the delay relay times out and its contacts close. When the contacts are closed, the two  $4\Omega$  resistors are shorted and normal power is supplied to the machine.

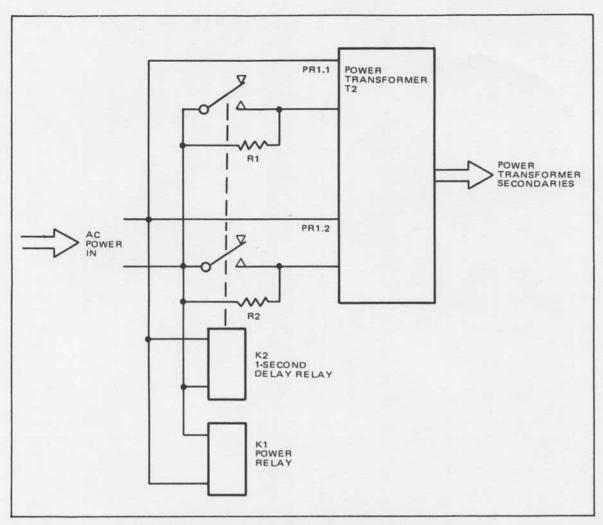
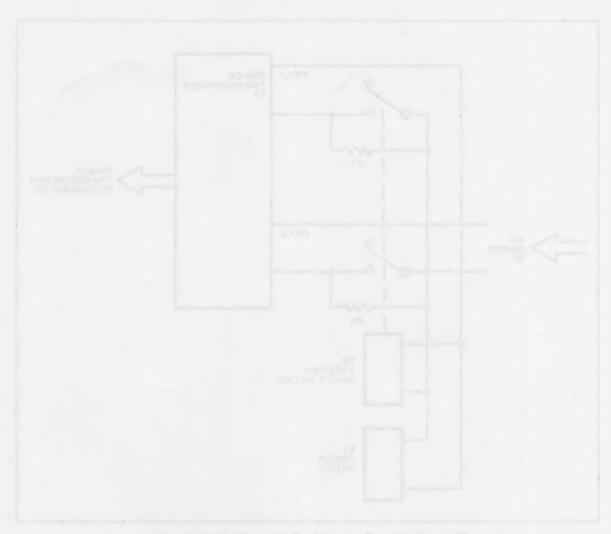


Figure 4-36. Power-Up Relay-Block Diagram



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## SECTION 5 MAINTENANCE

### 5-1 GENERAL

This section of the manual provides maintenance information for the ATR-116/124 Recorder/Reproducer. This information is grouped under five main headings: Overall Test Equipment Requirements, Preventive Maintenance, Alignment and Adjustments, Performance Tests, and Corrective Maintenance.

Under Overall Test Equipment Requirements, Table 5-1 lists test equipment (electronic and mechanical) for testing, adjusting, and maintenance of the ATR-116/124. Preventive Maintenance covers procedures for cleaning, demagnetizing, and lubrication.

Information grouped under Alignment and Adjustments includes procedures for the audio signal system and the tape transport. Information under the heading Performance Tests includes tests for checking tape tension, absolute tape speed accuracy, speed variation, operating level, signal-to-noise ratio, harmonic distortion, intermodulation distortion, and flutter. Corrective Maintenance covers procedures for head maintenance, troubleshooting, and component replacement procedures.

### CAUTION

DO NOT USE ANY FORM OF ABRASIVE LAPPING TAPE ON THE ATR-116/124 HEADS AS SERIOUS DAMAGE CAN OCCUR, VOIDING HEAD WARRANTY.

TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS, ALWAYS TURN RECORDER/REPRODUCER POWER OFF BEFORE REMOVING OR INSTALLING A HEAD ASSEMBLY, OR BEFORE REMOVING OR INSTALLING A PRINTED WIRING ASSEMBLY (PWA).

Table 5-1. Overall Test and Maintenance Equipment Requirements

Equipment Type	Suggested Model Used For Electronic checks an adjustments.	
DC Voltmeter - 20,000 Ω/V		

(Continued next page)

Table 5-1. Overall Test and Maintenance Equipment Requirements (Continued)

Equipment Type	Suggested Model	- response, and	
Low distortion oscillator/distortion test set	Sound Technology Model 1710A with intermodu- lation distortion option.		
Spectrum analyzer (plug-in)	Tektronix Model 7L5 (with model 7704 or equivalent main frame).	IARRA I	
Oscilloscope (dual trace)	Tektronix Model 465B	Head azimuth adjustment and signal system, tacho- meter and servo align- ment.	
Band limiting filter 30 Hz to 18 kHz	See Figure 5-29	Signal-to-noise measure- ment.	
ANSI A Weighted Filter	See Figure 5-30	Signal-to-noise measure- ment.	
Universal Noise Filter (optional)	See Figure 5-31	Signal-to-noise measure- ment.	
AC Voltmeter	HP400F	Reproduce equalization adjustment.	
2 in. flux loop	Ampex P/N 4020484-01	Performance check and electronic alignment.	
Flux loop equalizing amplifier	Ampex P/N 4020424-01	Performance check and electronic alignment.	
Head Preamp Test PWA	Ampex P/N 4051078-01	Head preamplifier align- ment.	
Tape Tension Gauge	Tentel PN T2-H20-ML (Ampex PN 1408151) or Tentel PN T2-H20-2 (Ampex PN 1408152)	Measuring tape tension.	
Head demagnetizer	Ampex P/N 4040575	Demagnetizing head stacks.	
Hand-held bulk demagnetizer	Any	Demagnetizing tape guides and other components in the tape path.	

Table 5-1. Overall Test and Maintenance Equipment Requirements (Continued)

Equipment Type	Suggested Model	Used For  Cleaning heads.  Lubrication of components.  Cleaning tape guiding components.  PURC timing alignment.  Flutter measurement and troubleshooting.  Tape speed and speed variation check.  Extends electronics assembly and pre-amp PW As for test.	
Head cleaner	Ampex P/N 4010823 or 087-007		
Lubricants	See paragraphs 5-9 and 5-10		
Isopropyl alcohol (approximately 92%)	Any		
Automatic record/play cycler (optional)	See paragraph 5-60		
Flutter meter	Micom Model 8100W with analyzer		
Frequency counter	Hewlett-Packard Model 5300A/5302A		
Extender board	Ampex P/N 40501052-01 and 4050800-01 (Supplied with recorder/reproducer)		

### 5-2 OVERALL TEST EQUIPMENT REQUIREMENTS

Electronic and mechanical test equipment suggested for use during testing, alignment, adjustment, and maintenance of the recorder/reproducer is listed in Table 5-1. Test equipment with equivalent or better specifications can be substituted for the equipment suggested in the table, e.g., Sound Technology 1510A.

### 5-3 PREVENTIVE MAINTENANCE

It is important that preventive maintenance, consisting of cleaning, demagnetizing, and lubrication procedures, be performed at the intervals recommended.

### 5-4 Cleaning

### 5-5 Tape Path Cleaning

Oxide particles from the magnetic tape tend to collect on components in the tape path. These oxide accumulations degrade the performance of the recorder/reproducer. The heads and all other components in the tape path should be cleaned after each eight hours of operation, or more frequently if visual inspection indicates cleaning is needed. Frequency of cleaning required depends greatly on the quality of tape in use.

#### CAUTION

WHEN CLEANING THE HEADS, USE HEAD CLEANER ONLY AND DO NOT USE METAL OR ANY TOOLS THAT COULD SCRATCH HEADS.

### Proceed as follows:

- STEP 1 Clean each head thoroughly with a cotton-tipped applicator dampened with Ampex Head Cleaner (Part No. 4010823 or 087-007).
- STEP 2 Clean all tape-guiding components, tension arms, tape timer wheel, and capstan with 92% (approximately) isopropyl alcohol. Do not allow alcohol to enter bearings.
- STEP 3 Clean scrape-flutter idler (on head assembly) with a dry cotton-tipped applicator.

### 5-6 Air Filter Cleaning

The lower fan panel air filters should be cleaned periodically, as often as required by ambient air quality. If filters are not properly cleaned, circulating air will heat up to a point where a thermal switch will open and cause the recorder to shut down. To clean filters, proceed as follows:

STEP 1 Remove the four screws (Figure 5-1) which attach lower fan panel to recorder.

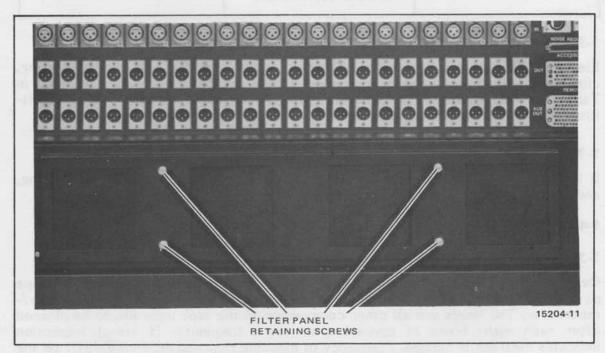


Figure 5-1. Air Filter Panel Retaining Screws

- STEP 2 Remove four filters from panel and clean them with compressed air.
- STEP 3 Wash filters with soap and water.
- STEP 4 Dry filters with compressed air and reinstall filters and panel.

### 5-7 Optical Devices

Optical devices on the ATR-116/124 seldom need cleaning and should not be cleaned on a routine basis. However, if required, clean the capstan tach disc and photo-sense devices as follows:

STEP 1 Clean capstan tach disc with a soft lint-free cloth moistened with glass cleaner or isopropyl alcohol. Instructions for removal of the capstan/tach assembly are given in this section of the manual.

### CAUTION

DO NOT USE ANY SOLVENTS, ALCOHOL, OR GLASS CLEANER OTHER THAN WATER, ON ANY LED OR PHOTO-SENSE DEVICE. TO DO SO CAUSES DAMAGE TO THE PLASTIC COVER.

STEP 2 Clean LEDs or any photo-sense device with a dry cotton-tipped applicator or, if necessary, an applicator moistened only with water.

### 5-8 Demagnetizing

The head should be demagnetized after each eight hours of operation, or as required.

### CAUTION

DO NOT REMOVE THE HEAD ASSEMBLY OR A PWA WITH POWER ON. TO DO SO CAUSES THE HEAD TO BECOME MAGNETIZED.

Heads and other components in the tape path can acquire permanent magnetization that degrades signal-to-noise, increases distortion, and partially erases high frequencies on recorded tapes. Use an Ampex Head Demagnetizer (Part No. 4040575), or equivalent to demagnetize components in the tape path.

### CAUTION

REMOVE RECORDED TAPE FROM THE VICINITY OF THE DEMAGNETIZER TO PREVENT ACCIDENTAL TAPE ERASURE.

### Proceed as follows:

- STEP 1 Turn equipment power off and remove any recorded tape near transport.
- STEP 2 Remove transport head cover assembly.
- STEP 3 Cover head demagnetizer tips with adhesive tape to prevent scratching head face.

- STEP 4 With demagnetizer at least three feet away from head assembly, connect demagnetizer to appropriate ac power source.
- STEP 5 Slowly move demagnetizer toward one head stack and lightly place demagnetizer tips to base of the stack straddling the head gap.
- STEP 6 Using a slow, even motion, move demagnetizer tips up and down entire face of stack several times. Then slowly withdraw demagnetizer.
- STEP 7 Repeat steps 5 and 6 for each head stack.
- STEP 8 Slowly move demagnetizer at least three feet from head assembly and then unplug the demagnetizer.

### 5-9 Scrape Flutter Idler Lubrication

The only item on the recorder/reproducer that requires periodic lubrication is the scrape flutter idler. Ultrasonically clean and then lubricate the scrape flutter idler once a year or after each 2,000 hours of operation.

### Proceed as follows:

- STEP 1 Remove head assembly from transport (see paragraph 5-71).
- STEP 2 Remove head shield (step 3, paragraph 5-72).
- STEP 3 Loosen scrape flutter idler retaining screw shown in Figure 5-2 and remove idler from head assembly base. Before removal, mark around base of idler yoke with relocate lines (Figure 5-2) to facilitate reinstallation.

#### Note

### Step 4 should be performed with care to prevent jewel bearing damage.

- STEP 4 Loosen the two allen-head bearing clamp screws (Figure 5-3) in yoke assembly. Slide two jewel-bearing holder assemblies out of yoke and remove idler.
  - a. Ultrasonically clean the two jewel-bearing holder assemblies and idler.
  - Lubricate each jewel-bearing holder assembly with Fluorogel 816 grease (Ampex Part No. 087-719).
  - c. Reassemble idler and jewelbearing holder assemblies into yoke and lightly tighten two bearing clamp screws.
- STEP 5 With upper and lower bearing clamp screws loose, set idler height (Figure 5-3) to 0.595 ±0.005 in. above yoke base. Lightly tighten lower bearing clamp screw.

- STEP 6 With upper bearing clamp screw still loose, remount idler onto head base plate with front and side of yoke even with the relocate lines on base plate (Figure 5-2).
- STEP 7 While pressing upper jewel bearing holder assembly toward idler with very light finger pressure, lightly tighten upper bearing clamp screw. Spin idler with finger; it should spin freely with no evidence of binding.
- STEP 8 Reinstall head shield (two allen-head screws) and install head assembly on to transport.

### 5-10 LUBRICATION

Table 5-2 provides a list of lubricants used where necessary on the recorder/reproducer and application instructions. Note that the capstan motor and tape timer bearings do not require relubrication. If these bearings are replaced with non-prelubricated bearings, use the grease suggested in the table. Except for the scrape flutter idler, which should be cleaned and lubricated after each 2,000 hours of operation, the other items shown in the table should be lubricated as required for proper operation.

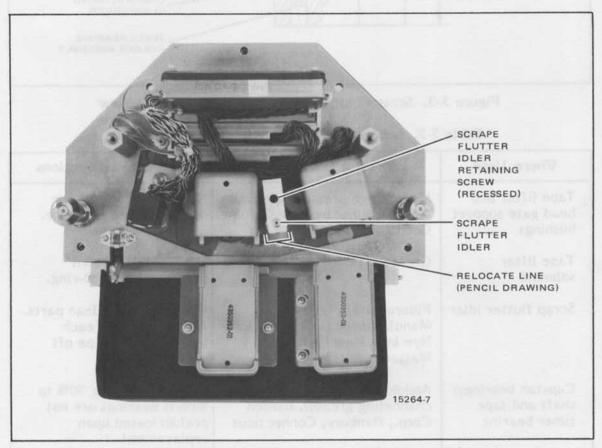


Figure 5-2. Scrape Flutter Idler Mounting Screw Location

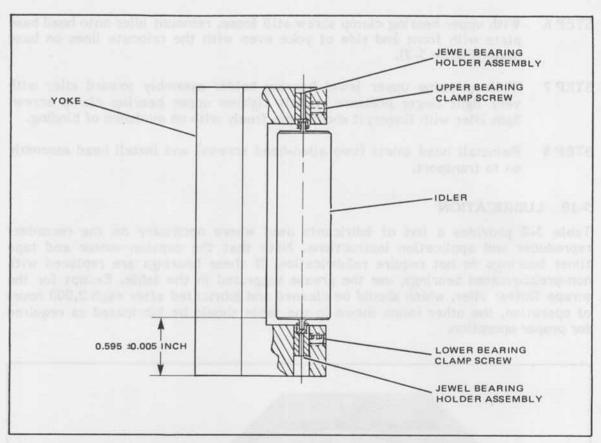


Figure 5-3. Scrape Flutter Idler, Side Cross-Section View

Table 5-2. Lubricants Used on Recorder/Reproducer

Where Used	Lubricant Description	Rub grease into entire surface of bushing bore.	
Tape lifter and head gate support bushings	MoS <sub>2</sub> , (high pressure grease). Manufactured by Dow Corning Corp., Midland, Michigan		
Tape lifter solenoid	Grease, STP	Use a small amount around solenoid O-ring.	
Scrap flutter idler	Fluorogel 816 (grease).  Manufactured by William F.  Nye Inc., New Bedford,  Massachusetts	Ultrasonically clean parts. Apply grease to each bearing bore. Wipe off excess.	
Capstan bearings; shaft and tape timer bearing	Andok C (general purpose channeling grease). Barden Corp., Danbury, Connecticut	Fill each bearing 30% to 40% if bearings are not prelubricated upon replacement.	

### 5-11 Tape Lifter Arm Bushings

The two tape lifter arm bushings have been permanently lubricated; however, if additional lubrication is required, proceed as follows:

- STEP 1 Remove head assembly (paragraph 5-72).
- STEP 2 Remove grip ring (Figure 5-4) on underside of lifter arm assembly.
- STEP 3 Remove roller, actuator arm, torque arm, and delrin washer.
- STEP 4 Remove lifter arm assembly.
- STEP 5 Rub MoS<sub>2</sub> high-pressure grease (Table 5-2) into bushing. It is not necessary to remove the bushing.
- STEP 6 Reinstall the tape lifter arm assembly in reverse order, observing the clearances noted in Figure 5-4.
- STEP 7 Reinstall head assembly.
- STEP 8 Perform steps 4 through 8 of the tape lifter arms adjustment procedure (paragraph 5-22).

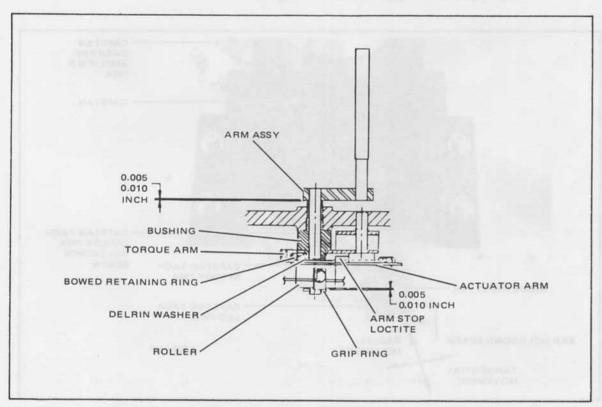


Figure 5-4. Tape Lifter Arm Assembly Cross Section

### 5-12 ALIGNMENT AND ADJUSTMENTS

### 5-13 Tape Transport Adjustments

### 5-14 Capstan Tach Sensor

See Figure 5-5. Use the following procedures to check the operation of the Capstan Tach Sensor PWA and Capstan Tach LED PWA; and, if required, adjust the position of the Capstan Tach Sensor PWA (steps 13 through 27). Normally an adjustment is required if the capstan motor "runs away" or if the Capstan Tach Sensor PWA or Capstan Tach LED PWA is replaced. Proceed as follows:

- STEP 1 Remove tape from recorder/reproducer.
- STEP 2 Remove head cover assembly by taking out the five mounting screws (Figure 5-6).
- STEP 3 Remove Capstan Servo PWA, set switch S1-2 of PWA to the service position by pressing the lower end of switch, and then reinstalling the PWA.
- STEP 4 Connect TP1 and TP2 of the Capstan Tach Preamplifier PWA (Figure 5-5) to inputs of a dual trace oscilloscope. Set oscilloscope for chop mode and trigger off either signal.

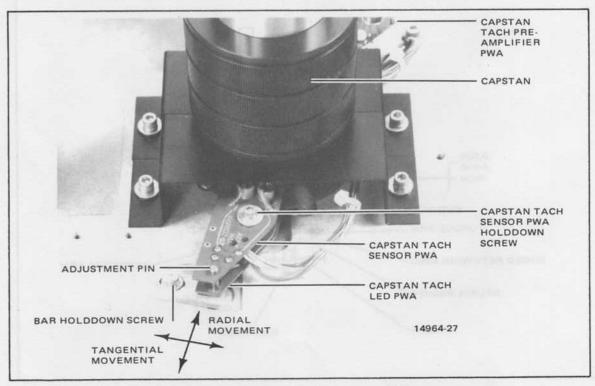


Figure 5-5. Capstan Tach Sensor Adjustment

- STEP 5 Apply system power and press PLAY. Amplitude of sinewave signals on scope should be approximately 15 Vp-p.
- STEP 6 Connect scope to tach 2 and tach 1 of Capstan Servo PWA. Adjust scope for chop mode and trigger scope from either one of two signals.
- STEP 7 The two signals should be 90° out of phase (Figure 5-7).
- STEP 8 Check for correct 90° phase relationship by pressing STOP and observe that capstan quickly stops.
- STEP 9 Press FAST FORWARD and observe that phase relationship of signals at tach 2 and tach 1 remains fairly constant as capstan accelerates to full speed.

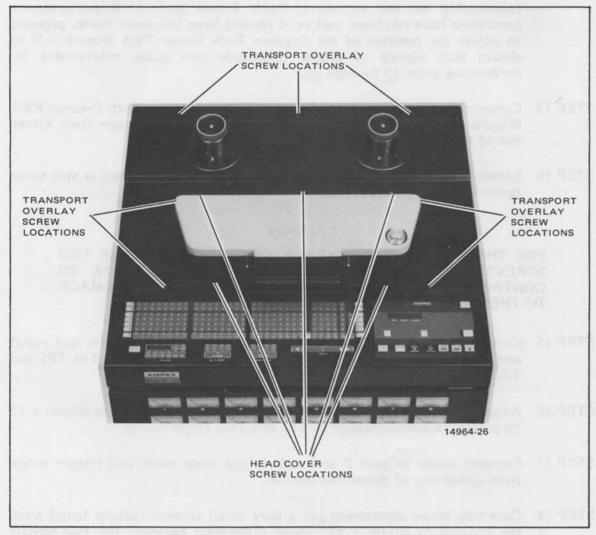


Figure 5-6. Removal of Transport Overlay Panel and Cover Assembly

#### Note

If scope chop rate is too slow to observe the phase relationship, switch scope to algebraic add mode to observe the waveform (Figure 5-7). The waveform shelves and spaces should be stable and not disappear or close.

- STEP 10 Press STOP and observe that capstan quickly stops.
- STEP 11 Repeat steps 9 and 10 in rewind mode.
- STEP 12 Proceed to step 25 if performance tests for amplitude, phase, and motion are correct; but if capstan runs faster when STOP is pressed, the Capstan Servo PWA may have a malfunction or the Capstan Tach Sensor PWA position may need to be adjusted to obtain the opposite 90° phase relationship of the signals at tach 2 and tach 1. If performance conditions have not been met or if repairs have just been made, proceed to adjust the position of the Capstan Tach Sensor PWA (Figure 5-5) to obtain tach signals of proper amplitude and phase relationship by performing steps 13 through 26.
- STEP 13 Connect dual trace scope to TPI and TP2 of Capstan Tach Preamp PWA (Figure 5-5). Adjust scope for chop mode and trigger scope from either one of two signals.
- STEP 14 Loosen two hold-down screws shown in Figure 5-5 so there is still some tension against lock washers.

#### CAUTION

FOR THE ADJUSTMENT THAT FOLLOWS, AND WHILE THE TWO SCREWS ARE LOOSE (STEP 15), DO NOT PERMIT PWA TO CONTACT THE ROTATING CAPSTAN TACHOMETER, AS DAMAGE TO THE TACHOMETER COULD OCCUR.

- STEP 15 Carefully move adjustment pin (Figure 5-5) tagentially (left and right) and radially (in and out) to capstan to obtain maximum output at TP1 and TP2 of the Capstan Tach Preamplifier PWA.
- STEP 16 Adjust potentionneters R4 and R5, on Capstan Tach PWA, to obtain a 15 Vp-p signal (approximately) at TP1 and TP2, respectively.
- STEP 17 Connect scope to tach 2 and tach 1. Use chop mode and trigger scope from either one of these two signals.
- STEP 18 Carefully move adjustment pin a very small amount radially (only) from the capstan to obtain a 90° phase difference between the two signals (Figure 5-7).

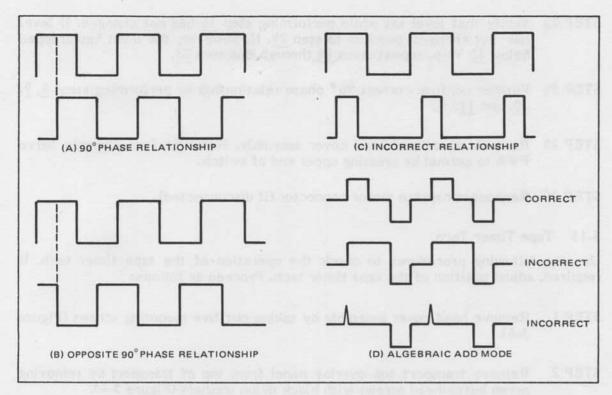


Figure 5-7. Tach 2 and Tach 1 Waveforms, Capstan Servo/Transport Control PWA

- STEP 19 Check for the correct 90° phase relationship by pressing STOP. If capstan quickly stops:
  - a. Tighten bar holddown screw (Figure 5-5)
  - b. Tighten Capstan Tach Sensor PWA holddown screw
  - c. Proceed to step 22; otherwise proceed with step 20.
- STEP 20 If capstan runs faster when STOP is pressed, press REWIND to stop capstan, then press PLAY. Readjust adjustment pin radially (only) for a 90° phase relationship opposite to that previously observed in step 19.

#### Note

Capstan may have to be held by hand to prevent runaway at high speed before proper phase is found. If desired, the capstan motor connector may be temporarily disconnected and capstan rotated by hand until the proper phase relationship is found.

- STEP 21 After opposite phase is established, first tighten bar holddown screw, then tighten the Capstan Tach Sensor PWA holddown screw (Figure 5-5).
- STEP 22 Connect scope to TP1 and TP2 of Capstan Tach PWA. Use chop mode and trigger off either signal.

- STEP 23 Verify that level set while performing step 16 has not changed. If level has not changed, proceed to step 24. If, however, the level has dropped below 12 Vp-p, repeat steps 14 through this step 23.
- STEP 24 Further confirm correct 90° phase relationship by performing steps 6, 9, 10, and 11.
- STEP 25 Remove power and head cover assembly. Reset S1-2 on Capstan Servo PWA to normal by pressing upper end of switch.
- STEP 26 Reconnect capstan motor connector (if disconnected).

### 5-15 Tape Timer Tach

Use the following procedures to check the operation of the tape timer tach. If required, adjust position of the tape timer tach. Proceed as follows:

- STEP 1 Remove head cover assembly by taking out five mounting screws (Figure 5-6).
- STEP 2 Remove transport top overlay panel from top of transport by removing seven buttonhead screws with black nylon washers (Figure 5-6).
- STEP 3 Thread tape on transport.
- STEP 4 Connect oscilloscope to TP3 on Offset Adjust PWA.
- STEP 5 Loosen tape timer tach adjusting screws (Figure 5-8).
- STEP 6 Engage servos and place transport in play mode.
- STEP 7 Adjust tape tach output for maximum output and most accurate sine wave by positioning tape timer tachometer about the tape timer tach encoder disc.

#### CAUTION

#### USE CARE TO AVOID BENDING TIMER TACH DISC.

- STEP 8 Repeat step 7 in fast wind or rewind mode. A further fine adjustment may be required.
- STEP 9 Tighten tape timer tach adjustment screws while monitoring tape timer tach output. The optimized tach position should not be changed while tightening adjustment screws.



Figure 5-8. Tape Timer Tachometer Adjustment

#### 5-16 Tension Arm Limits

### Note

The following procedure is identical for takeup and supply tension arms. Adjustments should be made on the Take-up and Supply Position Adjust PWAs as appropriate.

- STEP 1 Remove head cover assembly by taking out five mounting screws (Figure 5-6).
- STEP 2 Remove transport overlay panel from top of transport by removing seven buttonhead screws with black nylon washers (Figure 5-6).
- STEP 3 With no tape on transport, apply power and allow tension arm to rest at maximum excursion inward.
- STEP 4 Adjust R34 (Figure 5-9) on Position Adjust PWA so that DS1 lights.
- STEP 5 DS1 should go out at midposition of tension arm. Adjust R34 so that arm is allowed to return to its rest position; DS1 will come on at 1/4 in. to 3/8 in. from mechanical stop. Try several times to ensure that this happens.

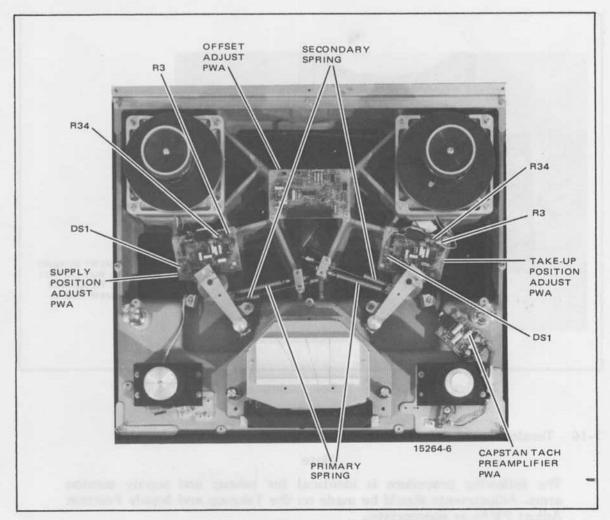


Figure 5-9. Tape Transport Adjust Locations

### 5-17 Tape-Tension Arms Postion Adjust

### Note

### This procedure must be repeated for each tension arm.

- STEP 1 Remove head cover assembly by taking out five mounting screws (Figure 5-6).
- STEP 2 Remove transport top overlay panel from top of transport by removing seven buttonhead screws and black nylon washers (Figure 5-6).
- STEP 3 Place tape on machine unthreaded.
- STEP 4 Set position adjustment R3 on Position Adjust PWA (a four-turn potentiometer) to midposition (Figure 5-9).

- STEP 5 Thread tape on recorder/reproducer, engage servos, and advance tape so there is equal tape pack on both reels.
- STEP 6 Place recorder/reproducer into stop mode.
- STEP 7 Adjust R3 so associated tape tension arm I-core is centered directly over E-core (Figure 5-10).

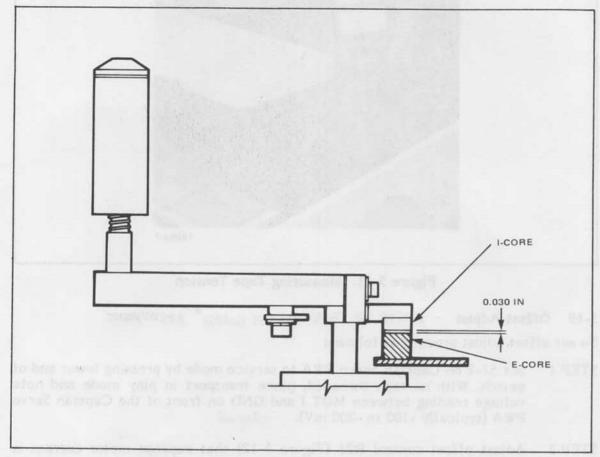


Figure 5-10. Tape Tension Arms I-Core/E-Core Locations

### 5-18 Tension Adjustment.

The adjustment procedure for the tape tension arms is identical for each arm. To adjust the tape tension arms, proceed as follows:

- STEP 1 With the I-core over E-core as in paragraph 5-17 step 7, refer to Figure 5-9; adjust collar on secondary spring so that spring is not extended and collar just contacts anchor plate.
- STEP 2 Adjust nut on spade bolt so tape tension (as measured with a tension meter), (Figure 5-11) is 9 oz ± 0.5 oz between reel and first tape guide with tape stopped.

House been advised that many users typically un tension higher (10-1202)5-17

Ampex 4890425-01

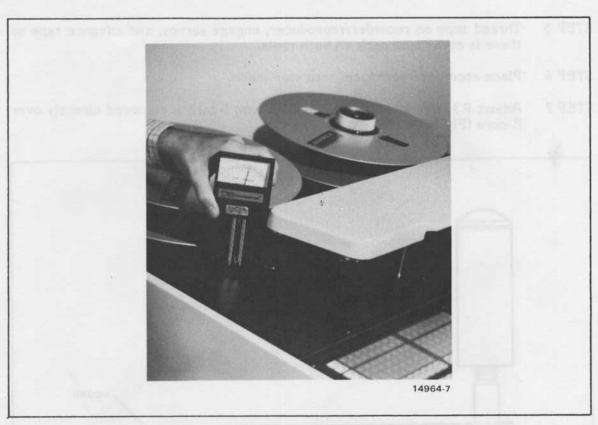


Figure 5-11. Measuring Tape Tension

5-19 Offset Adjust - REFER TO "AUTO-OFFSET BOARD" ADJUSTMENT
To set offset adjust proceed as follows:

- STEP 1 Set S1-2 on Capstan Servo PWA to service mode by pressing lower end of switch. With no tape threaded, place transport in play mode and note voltage reading between MOT I and GND on front of the Capstan Servo PWA (typically -100 to -200 mV). 210 mV
- STEP 2 Adjust offset control R21 (Figure 5-12) that capstan motor current is 200 mV more negative than that measured in step 1 when the transport is pulling tape (e.g., play mode). With R21 tolly CCW, best reading is -260 mV (depending on tope pack distribution). This may be Note normal.

This adjustment may be made without removing the transport trim. Refer to Figure 5-13 for location of the offset adjust (R21) access hole.

5-20 Tape Lifters Schem, Page 2)

Use these instructions to adjust tape lifter solenoid and the position of tape lifter arms.

SETUP #1: 3M 996, 30 ips

ROF Flux Ex 0 VU set at 520 nW/m.

(+9 over 185, reads "-6" VU with 250 nw tape)

Overblas 3/4 db at 1 khz (about 3db? at 10k).

Set lok Record BOR Using HF control, set LF PB ER For oals at locate,

gives \$1db from Sotte to ISK, Jour lob at 20K, Idb bump at 140 Hz.

SETUP # 2: 3M 996, 15 ips

ROF Flux for O VU set at 460 nW/m.

(+8 over 185, reads "-5" W with 250 nw tope)

Overbias (db at IKhz, +46b at 10k (3M recommendation)

(Set lok Record Ba using HF control, set (FPB Ba Fox Odb at looHz,

gives ±1 db from solte to 15k, down adb at 20k, 1db bunp at 70 140.

SBTUP #3: Ampex 456, 15 ips

ROF Flux Fox O VV set at 37.0 mw/m.

(+6 over 185, reads "-3" VU with 250 nw tape)

Overbias Yadb at 1khz (+3 db at 10k)

Set HF + CF EQ same as #2, gives ± 12 db SoHz-15k, Journ 126 at 20k,

bump at 70.

SETUP \$4: Ampex 456, 30 ips

ROF FUX FOX O VU Set at 370 NW/m.

(+6 over 185, reads "-3" yo with 250 nw tape)

Overblas 44 db at 1khz (+2 db at 10 k).

Set HF + LF Ea same as #1, gives = 126 from 50 Hz to 20K, same bumps.

NOTE: Using AGEA 468 on Ampex 456 settlings - second level at

Ik is about 1/2 db lower, low Requencies pretty Flat,

high Reguency boost of about 1 db above 10 K.

- 5-21 <u>Tape Lifter Solenoid.</u> When the tape lifter solenoid is energized or deenergized, trapped air between the plunger and solenoid housing is permitted to leak out slowly to provide slow and smooth tape-lifter action. Unless the tape lifter arms and cable linkage have been disassembled, the only adjustment that may be required is the solenoid air leak control. Proceed as follows:
- STEP 1 Remove left side trim panel (paragraph 5-84) to access tape lifter solenoid. Solenoid is located just below tape timer tachometer (Figure 5-14).
- STEP 2 Thread tape on transport.

### CAUTION

WHILE PERFORMING THE NEXT STEP, BE CAREFUL NOT TO SHORT THE SOLENOID POWER TERMINALS.

STEP 3 Adjust tape lifter solenoid air-leak screw, centered on end of solenoid, for fast and smooth tape lifter action when LIFT DEFEAT is alternately

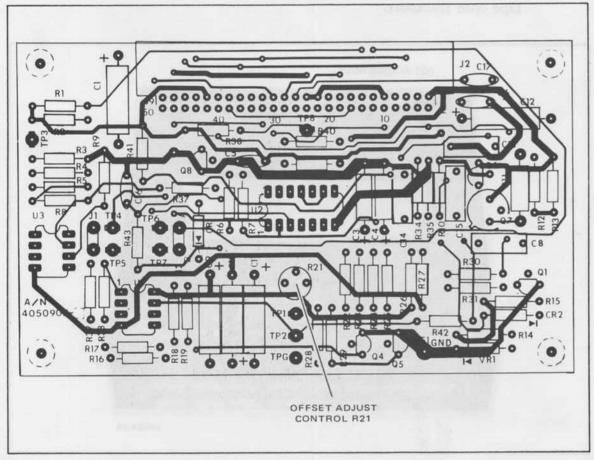


Figure 5-12. Tape Tension Offset Adjustment Control

pressed and released. The solenoid takes approximately 1-2 seconds to lift or retract tape. (Air-leak screw has a thread-locking device and is held in place by friction.)

STEP 4 Replace left side trim panel.

5-22 <u>Tape Lifter Arms.</u> Tape lifter arms must retract clear of the tape surface in stop and play/record modes (solenoid deenergized). The tape lifters can be individually adjusted to permit information on tape to be monitored by the reproduce or record head (Sel-Sync mode) while in fast forward, rewind, or spool modes. Tape lifter adjustment screws (Figure 5-14), adjusted with a 7/64 hex key, are located directly under the lifter posts when in the retracted position. (Note: the tape does not actually contact the heads in fast modes when the tape lifters are properly adjusted.)

If one or both tape-lifter arms contact the tape when solenoid is deenergized, perform steps  $\underline{1}$  through  $\underline{8}$ . If tape monitoring in fast forward, rewind, and spool modes is unsatisfactory, perform steps  $\underline{4}$  through  $\underline{8}$ . Proceed as follows:

STEP 1 Remove side trim panels (paragraph 5-85) and with power off, thread tape onto transport.



Figure 5-13. Offset Adjustment (R21) Access Hole

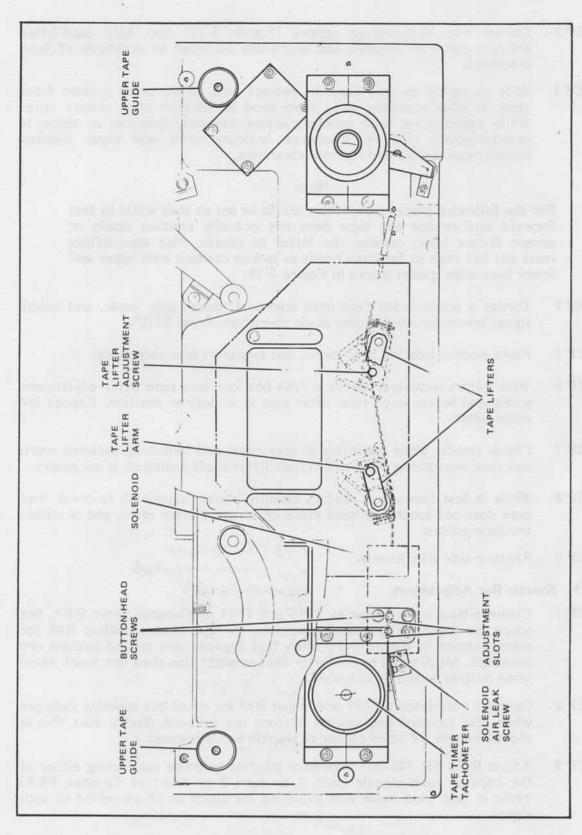


Figure 5-14. Tape Lifter Component Locations

- STEP 2 Loosen two button-head screws (Figure 5-14) that hold tape-lifter solenoid cover to solenoid and which are accessed at underside of tape transport.
- STEP 3 Slide assembly toward head to retract both lifter arms further from tape, or slide assembly away from head to advance arms toward tape. While maintaining tape tension, adjust assembly position so there is approximately 1/32 in. clearance between arms and tape. Tighten button-head screws and recheck clearance.

### Note

For the following steps, tape lifters are to be set so that while in fast forward and rewind the tape does not actually contact heads or scrape flutter idler, causing the latter to rotate. Also tape lifters must not lift tape so far from heads as to lose contact with upper and lower tape-edge guides shown in Figure 5-14.

- STEP 4 Thread a prerecorded tape onto transport, select play mode, and adjust signal levels for normal play mode operation. Press STOP.
- STEP 5 Place system into Sel Sync mode, and transport into play mode.
- STEP 6 With lifters actuated, insert a 7/64 hex key into tape lifter adjustment screw and rotate until tape lifter arm is in desired position. Repeat for other lifter.
- STEP 7 Check results while operating in play mode and switching between repro and sync monitoring modes. Readjust lifter shaft positions, if necessary.
- STEP 8 While in fast forward or rewind, visually inspect tape path to check that tape does not touch any head stack or scrape flutter idler, and is within the tape guides.
- STEP 9 Replace side trim panels.

# R48 = Shuttle Centor R49 = Shuttle Zero (offset) PKB = Shuttle Speed

### 5-23 Shuttle Bar Adjustment

- STEP 1 Connect dual trace scope to TP10 and TP11 on Capstan Servo PWA. Set scope for identical gain and ground on the two traces. Adjust R48 for wave pattern in Figure 5-15 when fast forward and rewind buttons are actuated. Set A equal to B. Verify that straight line does not touch ramp when neither button is actuated.
- STEP 2 Connect voltmeter to TP9 and adjust R49 for equal but opposite voltages when fast forward and rewind buttons are pressed. Verify that this is approximately 0V when center of shuttle bar is pressed.
- STEP 3 Adjust R161 for 350 in/s maximum winding speed by monitoring either of the capstan tach signals (tach 1 or tach 2 on front of Capstan PWA) while in fast wind mode and adjusting for about an 18-µs period of tach signal.

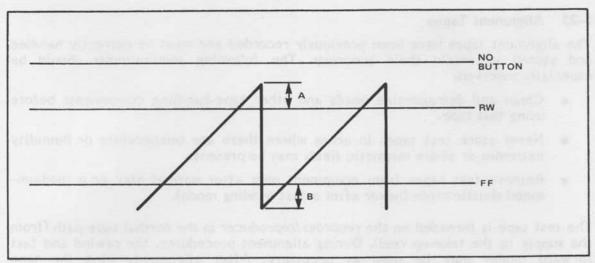


Figure 5-15. Shuttle Bar Adjustment - Waveform

### 5-24 Audio Signal System Alignment

The reproduce alignment procedure must be performed prior to the record alignment procedure. Reproduce alignment consists of setting high-frequency equalization of each channel, adjusting reproduce head racking, azimuth and phasing, and setting operating level of each channel. Record alignment consists of setting record head azimuth and racking, setting bias level, and setting record high-frequency and shelf equalization. Final reproduce low-frequency equalization is performed during record alignment. The alignment procedures are presented step-by-step in serial form for reproduce and record alignment of each channel. After the user is familiar with the procedures, it may be more convenient to perform the steps in parallel for each channel.

The basic recorder/reproducer internal electronics level is set to -5 dBm, regardless of the actual operating level flux level selected for use. For optimum performance, the use of Ampex 456 tape with an operating level of 370 nWb/m is recommended. (This level is 6 dB higher than the 185-nWb/m reference level on Ampex Standard Alignment Tapes.) Procedures are included in this manual for setting the operating level to 185 nWb/m, 260 nWb/m, and 370 nWb/m.

### Note

All voltage levels are expressed in dB referenced to 0.775V rms across  $600\,\Omega$ . Therefore, a level of zero dBm corresponds to 0.775V rms.

The ATR-116/124 provides four separate equalization setups that are selected on the secondary control panel. The VSO PWA contains a cluster of four LEDs that indicate which equalization setup is selected (as well as the indication provided by the switches on the secondary control panel). For a particular equalization adjustment, the illuminated LED on the VSO PWA indicates which set of controls on the audio PWA is to be adjusted. Thus, if LED 1 on the VSO PWA is lit, only the 1 controls on the Main Audio PWA are to be adjusted at that time.

### 5-25 Alignment Tapes

The alignment tapes have been previously recorded and must be correctly handled and stored to retain their accuracy. The following requirements should be especially observed.

- Clean and demagnetize heads and other tape-handling components before using test tape.
- Never store test tapes in areas where there are temperature or humidity extremes or where magnetic fields may be present.
- Remove test tapes from equipment only after normal play or a mediumspeed shuttle mode (never after a fast winding mode).

The test tape is threaded on the recorder/reproducer in the normal tape path (from the supply to the take-up reel). During alignment procedures, the rewind and fast forward modes may be used as necessary. After alignment, wind the tape completely on the take-up reel and then place the recorder/reproducer in a medium speed shuttle mode to wind the tape back on its original reel. Note that after extensive use, high-frequency tones on the alignment tape may drop as much as 2 dB, particularly at the slower tape speeds.

Operating level and reproduce frequency response can be checked with a standard alignment tape (Table 5-3). When using a standard alignment tape that is recorded for heads equal to the full width of the tape to check a system with heads less than full width, the response readings below approximately 10.0 kHz become progressively invalid as the frequency decreases. This is caused by the low-frequency fringing effect of the reproduce head. The reproduce head picks up additional flux beyond the track width of the head as the frequency decreases. This error, being wavelength dependent, becomes worse as the wavelength increases.

#### Note

Ampex alignment tapes listed in Table 5-3 have partial correction for fringing from 700 Hz to 15 kHz. Alignment tapes made by other manufacturers may have partial fringing correction. Check with the manufacturer.

Table 5-3. Ampex Test Tapes

Туре		Ampex Part Number	Time Constant (HF/LF)
NAB, 1 in.	7.5 in/s, 8-track	4690007	50 μs/3180 μs
NAB, 1 in.	15 in/s, full-track	4690005	50 µs/3180 µs
IEC (CCIR), 1 in.	15 in/s, full-track	4690031	35 μs/α
IEC/AES, 1 in.	30 in/s, full-track	4690048	17.5 µs/a
NAB, 2 in.	7.5 in/s, full-track	4690025	50 μs/3180 μs
NAB, 2 in.	15 in/s, full-track	4690024	50 μs/3180 μs
IEC (CCIR), 2 in.	15 in/s, full-track	4690035	35 μs/α
IEC/AES, 2 in.	30 in/s, full-track	4690047	17.5 μs/α

### 5-26 Using a Flux Loop

An accurate method of setting equalization involves the use of a flux loop driven by an audio oscillator in order to induce magnetic field in the reproduce head. The field produced by the flux loop may be equalized to simulate the short circuit flux/frequency response from an ideally recorded alignment tape. The response of a correctly equalized reproduce system to a correctly equalized flux loop is an almost constant output with frequency over the audio range of interest. However, the use of a flux loop does not disclose the following errors:

- Reproduce head low-frequency pole contour and secondary gap effect.
- · Reproduce head high-frequency gap loss.
- Effect due to head-to-tape contact, azimuth, or head racking errors.

The ATR-116/124 incorporates automatically selected preset equalization to correct for secondary gap rise at 7.5, 15, and 30 in/s. Therefore, at 7.5, 15, and 30 in/s, with the reproduce low-frequency and high-frequency equalizer controls correctly set, the actual flux-looped low-frequency response departs from a flat response by a specific amount depending on frequency. Figure 5-16 shows the correct response that should be obtained at 7.5, 15 and 30 in/s with the reproduce equalizers adjusted to match the equalization standard set on the equalized flux loop.

A recommended flux loop for use with the ATR-116/124 is the Ampex flux loop (Ampex Part No. 4020484) used with an Ampex flux-loop equalizing amplifier (Ampex Part No. 4040424). When an equalizing amplifier is not used, the flux loop may be passively equalized by use of a capacitor connected across the oscillator terminals to provide the high-frequency transition. The nominal capacitor value may be calculated by the following formula:

$$C = \frac{T(R_0 + R_1)}{R_0 \cdot R_1}$$

Where:

T =equalization transition time constant (seconds) (Table 5-3)

Rn =oscillator output resistance (ohms)

R<sub>1</sub> =flux loop dc resistance (ohms)

C =capacitance (microfarads)

Figure 5-17 shows the desired system response from an unequalized flux loop for the most common equalization standards. This assumes constant current through the flux loop when driven from a constant voltage source with an output resistance equal to or greater than zero ohms.

#### 5-27 Head Azimuth Phase

Head adjustment is required for record and reproduce head stack azimuth. Precision mounting of the record and reproduce head stack has eliminated the need for adjusting height and zenith. The azimuth adjustment is made by turning a hex screw (Figure 5-18) which causes a tapered gear to rotate underneath the head-stack precision plate. The azimuth adjustment is adjustable over a range of  $\pm$  10 minutes of arc.

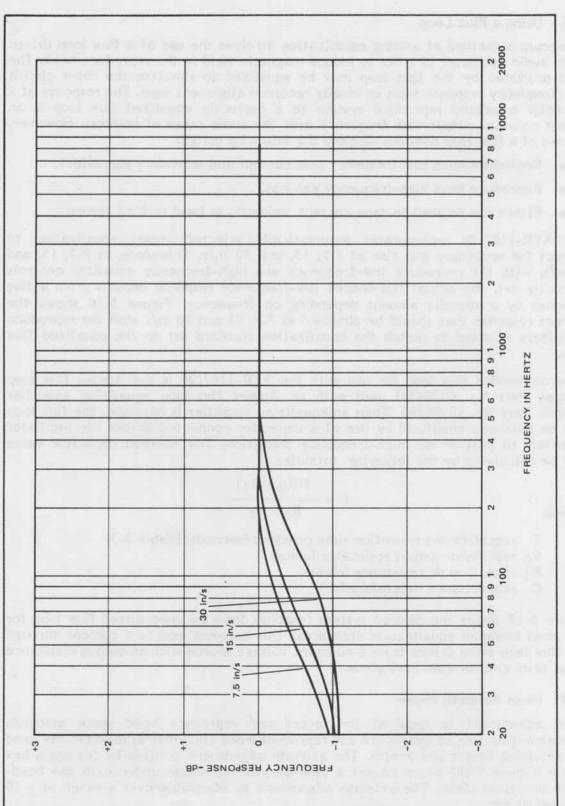


Figure 5-16. Equalized Flux Loop Response

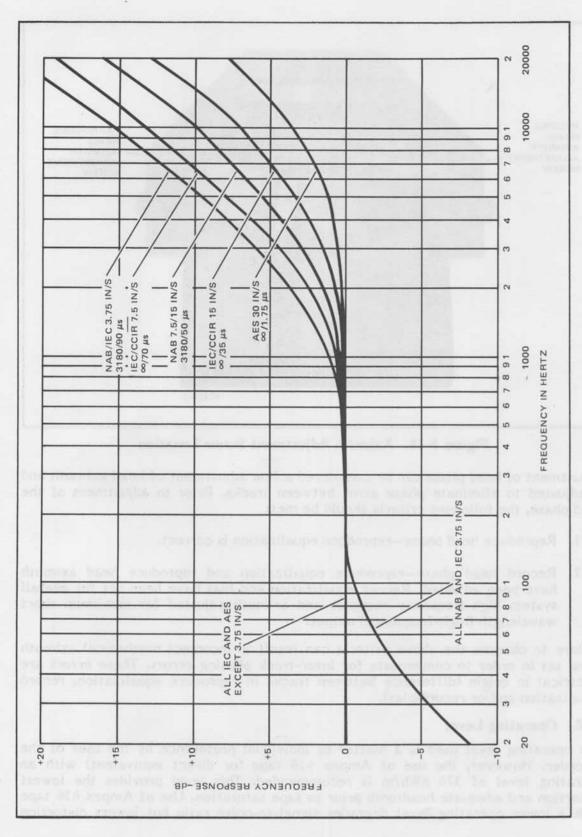


Figure 5-17. Reproduce Response From Unequalized Flux Loop

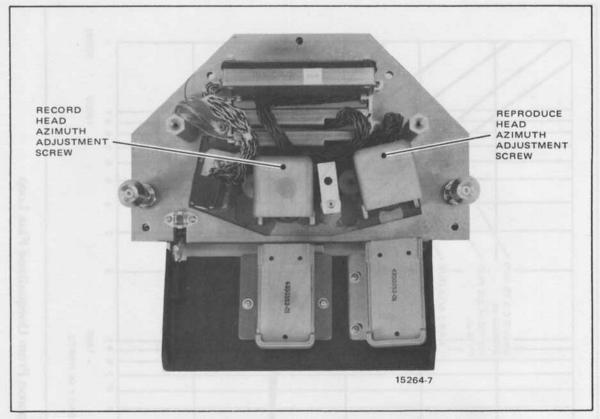


Figure 5-18. Azimuth Adjustment Screw Location

Adjustment of head phase can be considered a fine adjustment of head azimuth and is adjusted to eliminate phase error between tracks. Prior to adjustment of the head phase, the following criteria should be met:

- 1. Reproduce head phase-reproduce equalization is correct.
- Record head phase—reproduce equalization and reproduce head azimuth have been adjusted. Record equalization and bias have been set for overall system high-frequency response and azimuth adjusted for maximum short wavelength (high-frequency) output.

Failure to observe the above criteria can result in incorrect mechanical azimuth being set in order to compensate for inter-track phasing errors. These errors are electrical in origin (difference between tracks in reproduce equalization, record equalization and/or record bias).

### 5-28 Operating Level

The operating level used is a matter of individual preference by the user of the recorder. However, the use of Ampex 456 tape (or direct equivalent) with an operating level of 370 nWb/m is recommended. This level provides the lowest distortion and adequate headroom prior to tape saturation. Use of Ampex 456 tape with a lower operating level degrades signal-to-noise ratio but lowers distortion

1.0 kHz

700 Hz

Ik

and increases headroom. With other types of tape, other operating levels may be preferable. When using Ampex 406/407 tape, an operating level of not more than 260 nWb/m is recommended.

Operating level is set while reproducing a standard alignment tape of known short circuit fluxivity, and adjusting the recorder gain appropriately. In the case of the Ampex alignment tapes, reference levels of 185 nWb/m at 700 Hz are used. (Other manufacturers' alignment tapes have standard reference levels at 200 nWb/m or 250 nWb/m at 1.0 kHz, or 320 nWb/m at 1.0 kHz.) Table 5-4 shows the relative differences in level between Ampex reference level (185 nWb/m) and other reference levels in domestic and international use.

Relative Short Circuit Description Level Fluxivity Frequency Ampex reference level OdB 185 nWb/m 700 Hz or (standard operating 500 Hz level) Other U.S. reference +0.7 dB 200 nWb/m 1.0 kHz levels Elevated operating level +3 dB 250/260 nWb/m 1.0 kHz

+4.8 dB

+6 dB

+9 db

Table 5-4. Relative Operating Levels

If a full-width alignment tape is used to set reproduce gain, errors in absolute reproduce sensitivity can result due to the fringing effect. Error becomes more pronounced at the higher tape speeds and requires correction. Corrections must also be made when using a full-width alignment tape, because the reproduce core of ATR-116/124 is wider than the record core. Failure to make corrections can cause the recorder to fail distortion and frequency response tests.

320 nWb/m

370 Wb/m

520 now/m

To repeat: When checking frequency response using a full-track alignment tape, gains must be set higher than expected due to:

- Fringing error at the reference frequency (a wavelength-dependent condition).
- Wider reproduce core than record core (a constant factor dependent on track width).

Figures 5-19 and 5-20 show, respectively, calculated fringing response for the ATR-116 and ATR-124 reproduce heads. The constant reproduce core width correction factors are 0.6 dB and 1.0 dB, respectively, for the 16- and 24-track heads. Table 5-5 shows combined correction factors for selected tape speeds and

IEC reference level

with 456 tape

Recommended operating

level for ATR-116/124

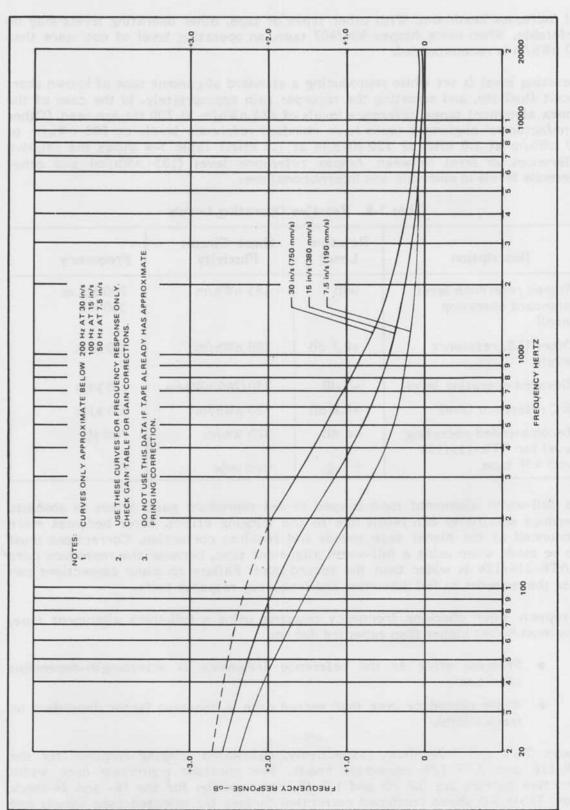


Figure 5-19. 16-Track (ATR-116) Reproduce Head Fringing Response

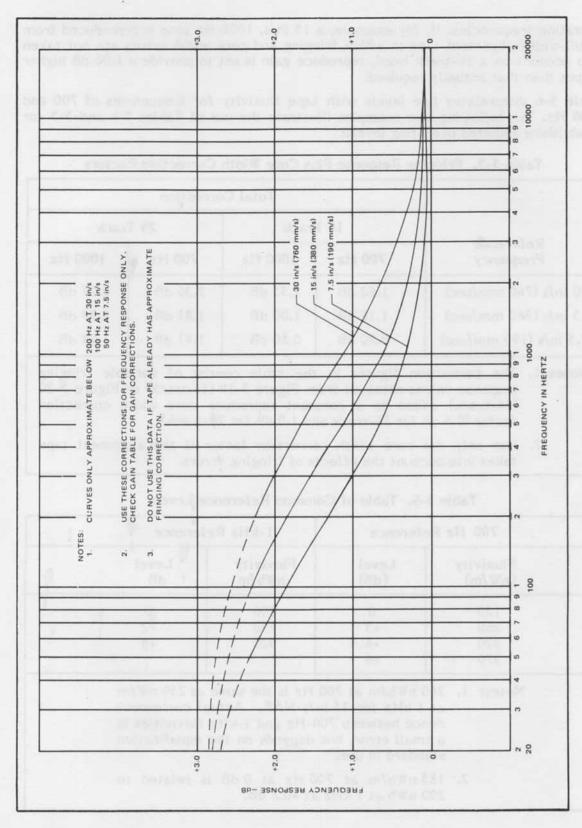


Figure 5-20. 24-Track (ATR-124) Reproduce Head Fringing Response

operating frequencies. If, for example, a 15 in/s, 1000-Hz tone is reproduced from a full-width alignment tape in which fringing and core width errors are not taken into account on a 16-track head, reproduce gain is set to provide a 1.00 dB higher output than that actually required.

Table 5-6 interrelates line levels with tape fluxivity for frequencies of 700 and 1000 Hz. The following two examples illustrate the use of Tables 5-4 and 5-5 for establishing required operating levels:

Table 5-5. Fringing Response Plus Core Width Correction Factors

		Total C	Correction	
2.4	16	Track	24 Track	
Reference Frequency	700 Hz	1000 Hz	700 Hz	1000 Hz
30 in/s (760 mm/sec)	1.62 dB	1.35 dB	2.36 dB	2.07 dB
15 in/s (380 mm/sec)	1.18 dB	1.00 dB	1.81 dB	1.59 dB
7.5 in/s (190 mm/sec)	0.90 dB	0.80 dB	1.41 dB	1.28 dB

- Notes: 1. The correction figures in the table consist of variable fringing response values obtained from Figure 5-19 (16-track) or Figure 5-20 (24-track) added to a constant reproduce core width correction factor (0.6 dB for 16-track and 1.0 dB for 24-track).
  - 2. Use only the core width correction factor if the alignment tape takes into account the effects of fringing errors.

Table 5-6. Table of Common Reference Levels

	700 Hz Reference		1-kHz Re	1	
	Fluxivity (nW/m)	Level (dB)	Fluxivity nWb/m	Level dB	9
3	185	0	200	0	0
	260	+3	250	+2	1 1
	320 370	+4.8	320	+4	

Notes: 1. 260 nWb/m at 700 Hz is the same as 250 nW/m at 1 kHz for 15 in/s NAB. Actual correspondence between 700-Hz and 1-kHz fluxivities is a small error, but depends on the equalization standard in use.

 185 nWb/m at 700 Hz at 0 dB is related to 200 nWb at 1 kHz at +0.7 dB. Example 1: A 370 nWb/m operating level is required on a 24-track system at 30 in/s. A standard Ampex reference tape is available (185 nWb/m with a relative level of 0 dB at 700 Hz).

- 1. Table 5-6 indicates that 370 nWb/m is 6 dB above 185 nWb/m.
- 2. If line output operating level is +4 dBm at a 0-vu meter reading for 370 nWb/m, it would be -2 dBm or -6 vu for 185 nWb/m.
- 3. However, fringing response plus core width correction factor must be added to the ideal output. According to Table 5-5, this is +2.36 dB.
- 4. The repro level is, therefore, set for a +0.36 (approximately 0.4) dBm output or -3.64 (approximately -3.6) vu.

Example 2: A 250 nWb/m operating level at 1 kHz is required on a 16-track system with output level set for +10 dBm at 0 vu. A tape, corrected for approximate fringing response, is available with a 200 nWb/m fluxivity at 15 in/s.

- 1. Table 5-6 indicates 200 nWb/m is 2 dB below 250 nWb/m.
- Because line output operating level is +10 dBm at a 0-vu meter reading for 250 nWb/m, it would be +8 dBm or -2 vu for 200 nWb/m.
- 3. However, only the core width correction factor must be added to ideal output since the fringing response has already been taken into account. According to Note 1 of Table 5-5, core width correction factor is +0.6 dB.
- 4. Repro level is, therefore, set for a +8.6 dBm output which would correspond to -1.4 vu.

## 5-29 Reproduce Equalization Adjustment

Reproduce equalization adjustment consists of setting the low- and high-frequency equalization of each audio channel, utilizing a standard alignment tape or flux loop. The more accurate method of setting equalization involves the use of a flux loop driven by an audio oscillator to induce flux into the reproduce head. Both methods of setting equalization are given in the procedures of (paragraphs 5-30 and 5-31). Before performing the alignment procedure, refer to the general discussion regarding the use of flux loops, paragraph 5-26.

#### Note

Where input and output line levels pertaining to the input/output circuits are stated, it is assumed that these circuits have been set to the factory-adjusted input and output line level of +4 dBm operating level (0 vu). If another value line input and output operating level is being used, the levels stated in the adjustment procedures should be amended by the amount of deviation from the +4-dBm operating level.

### CAUTION

TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS ON A PWA, ALWAYS TURN RECORDER/REPRODUCER POWER OFF BEFORE REMOVING OR INSTALLING THE PWA.

## 5-30 Reproduce Equalization Procedure Using an Alignment Tape

This procedure assumes use of an Ampex alignment tape and an operating level of 370 nWb/m. See also paragraphs 5-24, 5-25, and 5-28.

- STEP 1 Clean and demagnetize the head and other tape path components as described in paragraphs 5-3.
- STEP 2 Apply system power.
- STEP 3 Select appropriate transport tape speed.
- STEP 4 Select an equalization setup (EQ1, EQ2, EQ3, or EQ4) on secondary control panel. An indicator on VSO PWA corresponding to selected equalization lights.
- STEP 5 Connect ac voltmeter to one of the following output connectors:
  - a. If Audio Test PWA is not used, connect ac voltmeter to appropriate recorder/reproducer output connector, and select Audio PWA corresponding to channel being adjusted. (See paragraph 5-61 if the Audio Test PWA is used for this procedure.)

#### Note

For the Audio Test PWA, input bus, output bus, and aux connectors are fixed at 0 dBm for 0 vu  $\pm 1/2$  dB.

- b. If Audio Test PWA is used, connect ac voltmeter to appropriate connector on the Audio Test PWA handle.
- STEP 6 Thread appropriate alignment tape (Table 5-3) on transport.

#### Note

If a full track alignment tape is used to adjust a multitrack system, it may be necessary to correct for the fringing effect. Refer to fringing effect discussion in paragraph 5-25.

STEP 7 Place system in play mode and establish reference frequency level according to substep 7a or 7b:

#### Note

If using a full width alignment tape, increase the gain to compensate for fringing response and core width (Table 5-5) in substep 7a or 7b below.

- a. Using an ac voltmeter:
  - (1) 7.5 in/s Set REPR GAIN control (Table 5-7) so that ac voltmeter at the 700-Hz reference tone (-10 dB below 185 nW/m, first tone on tape) reads -16 dBm at the output of the Audio Test PWA or -12 dBm at the line output.
- (2) 15 or 30 in/s Set REPR GAIN control so that ac voltmeter at the 700-Hz reference tone (185 nW/m, first tone on tape) reads -6 dBm at the output of the Audio Test PWA or -2 dBm at the line output.
  - b. Using VU meters:
    - (1) 7.5 in/s Depress the +10 dB pushbutton switch on the secondary control panel. Adjust the REPR GAIN (Table 5-7) control for a reading of -6 on the VU meter.
    - (2) 15/30 in/s Adjust the REPR GAIN control for a reading of -6 on the VU meter.

Table 5-7. Audio PWA, Handle Adjustments, Reproduce Equalization

	albei reginst	Index No	Name	Function
GAIN 1 2 3	10	1	REPR GAIN	Adjusts recorder/reproducer reproduce level for equalization set-up EQ1 through EQ4.
1 1 2		2	REPR HF	Adjusts high-frequency reproduce equalization for equalization set-up EQ1 through EQ4.
1 1 2 LF 3		3	REPR LF	Adjusts low-frequency reproduce equalization for equalization set-up EO1 through EO4.
AUDIO 4	10 800 0	am ble g stofa g gelen	Pairenguenni Punctesticipe Parence conce	flux loop is used as induce an elect we purpose of adjusting released of posterior for a supersol of cragging 7-26. Proceed as follows:
			TOWN DISK	no stone box next expenses. 1 577

- STEP 8 While reproducing the highest frequency tone on the alignment tape (15 kHz at 7.5, 15, and 30 in/s), make a coarse adjustment by setting the reproduce head azimuth screw (Figure 5-18) for maximum output.
- STEP 9 While reproducing the 10-kHz tone, adjust appropriate HF reproduce equalizer control for the same level obtained in step 7; however, note that the fringing correction for 10 kHz is different from that for 700 Hz.

- STEP 10 While reproducing the 50-Hz tone, adjust appropriate LF reproduce equalizer control for the same level obtained in step 7 (Note: This is an approximate setting; final adjustment is made during overall record/reproduce alignment procedure.)
- STEP 11 Reproduce frequency response test tones on the alignment tape. Reproduce response should conform to tolerance shown in Table 5-8 for other than full-width alignment tapes. For full-width alignment tapes add the correction factors indicated in Table 5-5.
- STEP 12 Repeat steps 2 through 11 for other audio channels to be adjusted.

Table 5-8. Reproduce Frequency Response Tolerance

Speed	Tolerance ±0.5dB	Tolerance ±1.5 dB
30 in/s	200 Hz - 20 kHz	40 Hz - 30 kHz
15 in/s	100 Hz - 15 kHz	25 Hz - 20 kHz
7.5 in/s	100 Hz - 10 kHz	25 Hz - 15 kHz

Note: For full width alignment tapes add the correction factor indicated in Table 5-5.

STEP 13 Adjust operating level using instructions in paragraph 5-37.

### Note

Final adjustment of the reproduce low-frequency equalizers for optimum low-frequency response is accomplished during an overall record/reproduce alignment procedure given later in this section of the manual.

## 5-31 Reproduce Equalization Using a Flux Loop

A flux loop is used to induce an electromagnetic field into the reproduce head for the purpose of adjusting reproduce equalization. Before performing the alignment procedure, refer to the general discussion concerning the use of flux loops in paragraph 5-26. Proceed as follows:

- STEP 1 Remove tape and apply system power.
- STEP 2 Select a channel to be aligned and place channel in repro mode.
- STEP 3 Select appropriate system tape speed at transport control panel.
- STEP 4 Select an equalization setup (EO1, EQ2, EQ3, or EO4) by pressing appropriate pushbutton switch on secondary control panel. Note: Make certain equalization is set for appropriate tape speed.

- STEP 5 Connect ac voltmeter to one of following output connectors:
  - If Audio Test PWA is not used, connect ac voltmeter to appropriate I/O panel output connector.
  - b. If the Audio Test PWA is used, connect ac voltmeter to appropriate connector on the Audio Test PWA.
- STEP 6 Clip flux loop to reproduce head, and locate properly for maximum signal reading on ac voltmeter.
- STEP 7 If a flux-loop equalizing amplifier is used, select appropriate equalization time constant on amplifier (Table 5-3) and connect audio oscillator to amplifier input. Make sure amplifier is not overdriven so as to cause clipping, particularly of low frequency signals.

### Note

If the Ampex flux-loop equalizing amplifier is used, set SGC switch to OFF for  $7\pm$  in/s. Clipping of the amplifier may be checked by placing an oscilloscope across the ground input terminal of the amplifier and each terminal, in turn, of the differential output of the amplifier.

- STEP 8 If a flux-loop equalizing amplifier is not used, connect appropriate equalizing capacitor (paragraph 5-26) across audio oscillator terminals and connect flux loop (Ampex Part No. 4020484) to the oscillator.
- STEP 9 Set oscillator to 1.0 kHz.
- STEP 10 Apply system power and set oscillator level and/or flux-loop equalizer amplifier level so that ac voltineter reads -10 dBm at the output of the Audio Test PWA, or -6 dBm at the output connector.
- STEP 11 Change oscillator frequency to 15.0 kHz.
- STEP 12 Adjust appropriate HF reproduce equalizer control (Table 5-7) for same level obtained in step 10.
- STEP 13 Sweep oscillator through frequency range of 10 kHz to 20 kHz. The response should be within ±0.25 dB of the level at 10.0 kHz.
- STEP 14 Change oscillator frequency to 30 Hz.
- STEP 15 Adjust appropriate LF equalizer control for the same level obtained in step 10. If flux loop equalization amplifier is not used, see Figures 5-16 and 5-17 for LF setting required for each speed/equalization standard in use.

- STEP 16 Sweep oscillator through frequency range of 20 Hz to 20 kHz. The response should match curves in Figure 5-20 within ±0.25 dB (or match LF portion of Figures 5-16 and 5-17 if the low-frequency equalizing amplifier is not used).
- STEP 17 Repeat steps 1 through 16 for the other audio channels to be adjusted.

### Note

Final adjustment of the reproduce low-frequency equalizers for optimum low-frequency response is accomplished during an overall record/reproduce alignment procedure given later in this section of the manual.

## 5-32 Reproduce Head and Record Head Azimuth

The ATR-116/124 employs limited-range-adjustable azimuth on both record and reproduce head stacks. The available adjustment range, ±10 minutes of arc, is designed to permit compensation for incorrect azimuth recordings. It is not practical to set edge-to-edge phasing using amplitude peaking with a 2-inch system; therefore, head azimuth must be adjusted with great care to prevent errors. For reference, 10 minutes of arc azimuth error will give 3-dB amplitude loss at 15 kHz and 7.5 in/s; one minute of arc will give only 0.03-dB amplitude error under some conditions, but the same azimuth error of one minute of arc will give 420° of phasing error over a 2-inch tape width (or 210° error at 15 kHz and 15 in/s). For this reason, it is unlikely that two reproduce alignment tapes will agree in phase within less than 0.25 minutes of arc or 26° at 15 kHz and 15 in/s across a 2-inch tape. Alignment tapes should, therefore, be used only as a local best reference for establishing a reasonable average azimuth setting for the reproduce head. The record head azimuth should be set normally while reproducing a recording being made on the record head. In addition to the above factors, failure to properly and uniformly adjust reproduce equalization and/or record bias and equalization can cause electrical interchannel phase errors of larger magnitude than 0.5 minutes of arc static mechanical error.

## 5-33 Reproduce Azimuth/Phase Procedure

#### Note

When system is connected to a monitoring console, it is possible to sum all channel outputs and monitor the resultant summed signal on a level meter. If this is done, omit steps 7 through 10 by reproducing the highest alignment tape frequency and adjusting the reproduce head azimuth for maximum indicated output; then perform steps 11 and 12.

- STEP 1 Clean and degauss head and install reproduce alignment tape on system.
- STEP 2 Wind to highest frequency section.
- STEP 3 Adjust repro azimuth adjustment screw (Figure 5-18) for maximum head output on highest frequency section as observed on VU meters.

- STEP 4 Check and, if necessary, adjust reproduce equalization (paragraph 5-30 or 5-31).
- STEP 5 Connect the channel 1 output to one channel of a dual trace oscilloscope and connect highest channel (16 or 24) to other oscilloscope channel. Set oscilloscope to trigger from one channel only. (If Audio Test PWA is used for this test, refer to paragraph 5-61 for usage.)
- STEP 6 Ensure that neither oscilloscope channel is inverted (temporarily connect both oscilloscope inputs to a single signal source).
- STEP 7 Reproduce a frequency from alignment tape not greater than 250 Hz at 7.5 in/s, 500 Hz at 15 in/s, and 1 kHz at 30 in/s. Adjust reproduce head azimuth to minimize phase error.
- STEP 8 Remove line output connector from channel 16 or 24 and monitor channel 2 line output. Reproduce the highest frequency on alignment tape.
- STEP 9 Adjust reproduce azimuth to minimize phase error.
- STEP 10 Remove line output connector from channel 2 and monitor channel 4 line output. Adjust reproduce azimuth to minimize phase error.
- STEP 11 Repeat the preceding step using channels 1 and 8, then channels 1 and 16, and finally channels 1 and 24. Use progressively finer adjustments.
- STEP 12 Check adjustment by reproducing alignment tape in order of ascending frequency. Note that no phase reversal occurs. If phase reversal occurs, repeat steps 8 through 11.

## 5-34 Record Head Azimuth/Phase Procedure

- STEP 1 Ensure reproduce equalization (paragraphs 5-29 to 5-31) and reproduce azimuth phase (paragraphs 5-32 and 5-33) are correct.
- STEP 2 Record and reproduce a 15-kHz signal and coarsely adjust record head azimuth adjustment screw (Figure 5-18) for maximum reproduced output.
- STEP 3 Ensure bias and record equalization are correctly adjusted for all channels (paragraphs 5-39 through 5-47).
- STEP 4 Connect a dual trace oscilloscope to monitor channel 1 line output and that of the highest channel (16 or 24). Set oscilloscope to trigger from one input only.
- STEP 5 Connect an audio oscillator to all channel inputs (if Audio Test PWA is to be used, refer to paragraph 5-61 for usage).

- STEP 6 Set oscillator for a frequency of 250 Hz at 7.5 in/s, 500 Hz at 15 in/s, or 1 kHz at 30 in/s. Place system in record on all channels and adjust oscillator for reproduced 0-vu meter indications. Select input/all and check for no phase inversion on the oscilloscope. Select repro/all.
- STEP 7 Adjust record head azimuth to minimize observed phase errors.
- STEP 8 Increase oscillator frequency slowly to 15 kHz. If any phase errors become apparent, readjust record azimuth to minimize average phase errors.
- STEP 9 Check adjustment by sweeping oscillator frequency from 1 kHz through 15 kHz. No phase reversal should occur. Momentary phase reversal may occur on peak excursions at 7.5 in/s, but average phase error should be zero.
- STEP 10 Finally, check channels 2 though 16 or 24 by monitoring the phase of each in turn compared to channel 1 at 15 kHz. No phase reversals should occur.

## 5-35 Racking Checks and Adjustments

Racking Adjustments (tape wrap optimization) should not normally be done unless a head stack has been removed or replaced from the baseplate assembly. For merely checking head stack racking, perform steps  $\underline{6}$ ,  $\underline{7}$ ,  $\underline{8}$ ,  $\underline{10}$ , and  $\underline{11}$  of paragraph 5-36, without making any adjustments.

It should be noted that if a head is racked away from optimum, a resulting reduction of head biasing will cause a rise in the recorded signal level until spacing caused by the misracking becomes dominant. Consequently a false peak in output can be interpreted to be the correct racking position.

The reproduce head racking may be set during overall simultaneous record/reproduce, but any attempt to verify the correct position by momentarily
increasing tension may cause record head irregularities which could be incorrectly
interpreted as reproduce racking error.

## 5-36 Racking Adjust Reproduce/Record Procedure

#### Note

If user desires only to check head stack racking, steps 6, 7, 8, 10, and 11 should be performed, making no adjustments.

### CAUTION

THE FOLLOWING RACKING PROCEDURE SHOULD BE DONE AS SOON AS POSSIBLE WITH NEW HEAD STACKS TO MINIMIZE ANY SET IN HEAD SURFACE WEAR IN AN INCORRECT POSITION.

- STEP 1 With an allen wrench, rotate racking screw (Figure 5-21) clockwise until reproduce head gap moves toward supply side. Mechanically set racking in center of its apparent mechanical adjustment range.
- STEP 2 Repeat for record head.
- STEP 3 Place a 15-in/s alignment tape on machine and adjust reproduce head azimuth for a maximum indicated output in the monomix mode (all channels equally combined) on the 15-kHz tone.
- STEP 4 Rock racking screw about its initial setting and adjust it coarsely for maximum uniform output across all channels.
- STEP 5 Repeat steps 3 and 4 for record head in the Sel Sync mode.
- STEP 6 Place a roll of 456 tape on recorder and record at 30 kHz and 15 in/s on all channels. If necessary, decrease appropriate master bias in order to optimize output amplitude.
- STEP 7 Record for at least three minutes, making no adjustments.

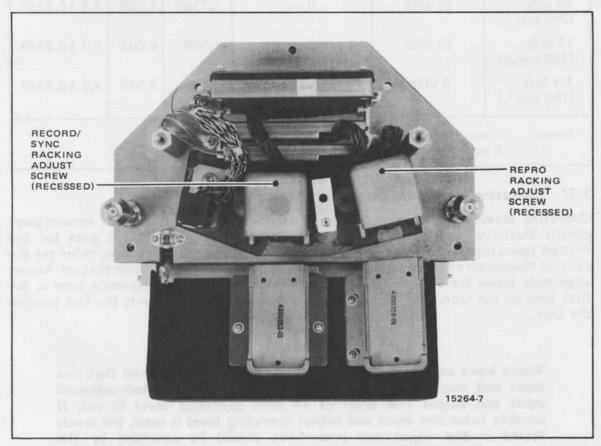


Figure 5-21. Racking Adjustment Screw Locations

- STEP 8 Rewind tape and replay recording. Adjust reproduce azimuth for maximum monomix output. Operate +10-vu meter sensitivity switch if needed.
- STEP 9 Carefully adjust racking to produce simultaneous maximum output on all channels.
- STEP 10 Momentarily increase holdback tension and note that no channel output increases by more than 0.2 dB. No increase is normal.
- STEP 11 Repeat steps 8 through 10 for the Sel Sync mode.
- STEP 12 Set master bias adjustment for proper level of overbias. See Table 5-9 and paragraph 5-41, step 13.

Table 5-9. Recommended Bias Point

Tape Speed	Frequency For Overbias	Record Level For Equalization and Overbias	Ampex 456	3M 250	AGFA 468
30 in/s (760 mm/s)	20 kHz	.0 vu	4.75dB	4.0dB	5.5 ±0.25dB
15 in/s (380 mm/s)	10 kHz	0 vu	4.0dB	4.0dB	4.5 ±0.25dB
7.5 in/s (190 mm/s)	5 kHz	-10 vu	3.0dB	3.5dB	4.0 ±0.25dB

Note: 0 vu = 370 nWb/m for Ampex 456

0 vu = 260 nWb/m for 3M 250 and AGFA

## 5-37 Operating Level Adjustment

Operating level is set by reproducing a standard alignment tape of known short circuit fluxivity, and adjusting the recorder/reproducer reproduce gain for the desired operating level. Prior to performing the alignment procedure, refer; to the general discussion concerning operating level, paragraph 5-28. Note that on Ampex alignment tapes for 15 and 30 in/s, the 185-nWb/m, 700-Hz reference tone is the first tone on the tape. For 7.5 in/s, the 185-nWb/m, 700-Hz tone is the last tone on the tape.

### Note

Where input and output line levels are stated, it is assumed that line input and output amplifiers have been set to the factory-adjusted input and output line level of +4 dBm operating level (0 vu). If another value line input and output operating level is used, the levels stated in the adjustment procedures should be amended by the amount of deviation from the +4 dBm operating level.

### CAUTION

IF OPERATING LEVELS OF LESS THAN 185 nWb/m ARE USED IN CONJUNCTION WITH HIGHER OPERATING LINE OUTPUT LEVELS, +8 dBm=0 vu, THEN WHEN REPRODUCING RECORDINGS ON AMPEX 456 OR SIMILAR HIGH OUTPUT TAPES, MIDBAND ELECTRONICS CLIPPING OF THE LINE OUTPUT AMPLIFIER CAN OCCUR PRIOR TO TAPE SATURATION. AMPEX 456 TAPE SATURATES AT ABOUT 20.5 dB ABOVE 185 nWb/m MIDBAND.

## 5-38 Fluxivity Operating Level Adjustment

- STEP 1 Clean and demagnetize heads and other tape path components as described in paragraph 5-3.
- STEP 2 Ensure equalization selectors on secondary control panel are programmed as desired and select EQ as desired.
- STEP 3 Select REPRO/ALL and select system tape speed.
- STEP 4 Connect an ac voltmeter to one of the following output connectors:
  - a. If Audio Test PWA is not used, connect voltmeter to the appropriate recorder output I/O panel output connector.
  - b. If Audio Test PWA is used, connect the voltmeter to the appropriate connector on Audio Test PWA.

#### Note

For the Audio Test PWA, input bus, output bus and aux connectors are fixed at 0 dBm for 0 vu ±1/2 dB.

- STEP 5 Thread appropriate alignment tape on transport and engage servos.
- STEP 6 While reproducing the 700-Hz, 185-nWb/m tone:
  - Adjust appropriate repr gain 1, 2, 3, or 4 control for the level/-fluxivity relative to 0 dB for 185-nWb/m fluxivity (Table 5-6). E.g., for a 370-nWb/m level: -6 dBm at one of the Audio Test PWA output connectors or VU meter and -2 dBm (see note following paragraph 5-37) at the line output connector.
  - b. If using a full width alignment tape, increase gain to compensate for fringing response and core width in accordance with Table 5-5.

### 5-39 Bias Normalizing

The ATR-116/124 uses a biasing system that permits all channels to be adjusted from any one of four master bias potentiometers which are located on the VSO PWA.

To enable this to work correctly for any one head assembly, the bias in each individual channel must be set precisely (i.e., normalized). Failure to do this will prevent adjustment of the master bias control for creating uniform bias conditions for each separate channel. Additionally, inconsistent biasing from channel to channel may cause apparent interchannel phasing errors, particularly at shorter wavelengths; however, once adjustment is performed and normalization is correct, then all further bias adjustments need only be performed using the relevant master bias (1-4) control.

The accuracy with which the different channels track each other after normalization depends on:

- · Bias normalizing being set at the same recorded fluxivity.
- Bias normalizing being done over a section of tape which has great uniformity.

The first condition is satisfied by setting the reproduce gain and equalization accurately for all channels. The second condition is met by using only a short length of tape and by using the looping capability of the SPSTC or MPSTC to ensure that the length of tape used is consistently the same for adjustment of each channel.

## 5-40 Preliminary

- STEP 1 Ensure that line input/output sensitivities are correctly set (paragraphs 5-56 and 5-58).
- STEP 2 Ensure that correct reproduce equalization and reproduce gain (paragraphs 5-29 through 5-31) adjustments have been accomplished.
- STEP 3 Remove system power and place VSO PWA on an extender board.
- STEP 4 Reapply system power and monitor pin 19 on the PWA with an oscilloscope.
- STEP 5 Adjust appropriate master bias (1-4) control for 6 Vp-p. The value of the master bias set here assumes use of a medium coercivity tape such as Ampex 406/407 or 456. High coercivity tapes should have bias voltages set at 8.5 Vp-p.
- STEP 6 Remove system power and replace the VSO PWA.

## 5-41 Bias Normalizing Procedure

Note

It is recommended that bias normalizing be performed at 15 or 30 in/s.

- STEP 1 Install a reel of bulk degaussed tape of the type to be used at the speed/equalization combination selected (for 7.5 in/s, press the VU meter +10 dB switch). Engage servos.
- STEP 2 Connect audio oscillator to all channel inputs (or connect to Audio Test PWA input and select all mode).
- STEP 3 Refer to Table 5-9 for overbias value relevent to tape and speed in use.
- STEP 4 Set oscillator to appropriate frequency indicated in Table 5-9, and adjust oscillator level to be lower than line input operating level (0 vu) by amount of overbias selected (for 7.5 in/s, use a level 10 dB lower than 0 vu). Normally, 0 vu is +4 dBm at line input and is always 0 dBm at input of the Audio Test PWA.
- STEP 5 Place all channels in record mode and select repro monitoring.
- STEP 6 Set cue point on tape at start of recording. (If MPSTC is used, set record end point at 2 minutes later than record/start and establish auto record looping.)
- STEP 7 Adjust channel 1 bias to normalize to maximum reproduced output signal as seen on channel 1 VU meter.
- STEP 8 Adjust appropriate record gain (1, 2, 3, or 4) as necessary to keep VU meter indication on scale.
- STEP 9 Finely adjust bias value to maximize output with VU meter indicating between ±1 vu.
- STEP 10 Set record gain to place VU meter indication at 0 vu.
- STEP 11 Increase channel bias normalize adjustment clockwise until VU meter reading has dropped by amount of overbias required.
- STEP 12 Repeat steps 7 through 11 for all remaining channels.

### Note

If bias normalize adjustment causes more than a 10-dB change in channel output from the initial adjustment, it may be necessary to recheck adjustment of adjacent channel.

If system has SPSTC only, do adjustments for 2 minutes maximum and then establish a play loop. If system has MPSTC, preestablish a 2-minute record loop. Failure to do so will result in poor interchannel bias tracking.

- STEP 13 When all channels have been adjusted, all VU meters should indicate a negative reading corresponding to amount of overbias selected. To verify correct normalizing, adjust appropriate master bias control counterclockwise to achieve peak output. All channels should peak simultaneously.
- STEP 14 If, at this time, any channels show a marked departure from uniformity, leave master bias set for maximum output for majority of channels and check channel bias levels. Relevel and readjust on only those channels necessary for maximum VU meter output. Master bias should then be turned clockwise until amount of overbias is seen on VU meters.

This completes normalizing procedure. No further adjustment of individual channel bias potentiometers should be necessary unless the record head is changed, a different head assembly is utilized, or an Audio PWA is exchanged. Other equalization positions and speeds can be biased independently by using appropriate master bias adjustment.

### 5-42 Record Alignment

Record equalization on the ATR-116/124 is set independently on any of the four equalizers at any of the transport speeds. The procedure involves setting master bias for the equalizer, record equalizers, and record gain. In addition, the procedure includes adjustment of low-frequency reproduce gain.

Two separate methods are given: Method I uses a normal sinewave audio signal generator, Method 2 uses a square wave generator and oscilloscope. The first procedure aligns the equalizers in the frequency domain while the second procedure gives the best balance between frequency domain response and transient time domain response.

Prior to record equalization adjustment, it will be necessary to have correct calibration of the input/output levels, a complete and accurate reproduce equalization and gain adjustment, and careful adjustment of bias normalizing for all channels. If these steps are not taken, erroneous frequency and time domain response will result and apparent phase error between channels will not be close to residual head gap scatter, but will become dominated by differences in bias and equalization.

Table 5-9 gives recommended overbias values for Ampex 456 tape as well as recommendations for two other commonly used tapes. Recommended biasing points have been chosen for minimum third harmonic distortion and modulation noise with high-frequency compression as a secondary factor.

Both procedures given below assume that all channels are being adjusted; however, to adjust a single channel, use the same procedures omitting those steps applicable to more than one channel.

## 5-43 Preliminary

- STEP 1 Ensure that system input level is set correctly (paragraph 5-56).
- STEP 2 Ensure that reproduce equalization (paragraph 5-29) and system output level (paragraph 5-58) are set correctly.
- STEP 3 Ensure reproduce head azimuth is set correctly (paragraph 5-32).

#### Note

Record alignment is performed at levels up to but not exceeding those in Table 5-10.

STEP 4 Connect a signal generator to all line inputs or use the Audio Test PWA input in the all mode (paragraph 5-61).

Table 5-10. Overall Record/Reproduce Procedure Frequency Response Limits for Ampex 456 Tape

Tape Speed	Response	Frequency	Level
30 in/s	± 0.75 dB	200 Hz - 20 kHz	0 vu
(760 mm/s)	± 2 dB	40 Hz - 30 kHz	
15 in/s	± 0.75 dB	100 Hz - 15 kHz	0 vu
(380 mm/s)	± 2 dB	25 Hz - 20 kHz	
7.5 in/s	± 0.75 dB	100 Hz - 10 kHz	-10 vu
(190 mm/s)	± 2 dB	25 Hz - 15 kHz	

## 5-44 Bias Normalization Check and Master Bias Adjustment

- STEP I Place a roll of bulk degaussed tape (of the type to be used) on transport. Engage servos.
- STEP 2 Select desired tape speed and equalization setup on secondary control panel.
- STEP 3 Select transport speed desired.
- STEP 4 Place all channels in record (READY/ALL then PLAY/RECORD).
- STEP 5 Select INPUT/ALL.
- STEP 6 Set the signal generator to 1 kHz and adjust the generator input level to give a 0-vu indication on VU meters.

- STEP 7 Select REPRO/ALL.
- STEP 8 On VSO PWA adjust master bias for selected equalization until a maximum output signal is obtained on all channels.
- STEP 9 Change oscillator frequency to that indicated in Table 5-9 for speed in use. Reduce oscillator level by amount of overbias indicated in overbias column of Table 5-9. Select INPUT/ALL to do this. For 7.5 in/s, reduce the level another 10 dB and press the +10-dB VU meter switch on secondary control panel.
- STEP 10 Select REPRO/ALL.
- STEP 11 Adjust master bias for selected equalization for maximum indicated output on any selected channel.
- STEP 12 Adjust the record head azimuth (paragraph 5-34) if required to further maximize output.
- STEP 13 Adjust record gain (Table 5-11) for the selected equalization on each channel in turn to acquire a 0-vu indication.

Table 5-11. Audio PWA, Handle Adjustments, Bias/Record Equalization

D vo	_		Index No.	Name	Function
BIAS		1	1	BIAS	Normalize record bias.
REC	1 2 3	-2	2	REC GAIN	Adjusts recorder/reproducer record level for equalization setup EO1 through EO4.
	1 2		3	REC HF	Adjusts record high-frequency equalization for equalization setup EQ1 through EQ4.
HF	3 4	(3)	4	REC SHLF	Adjusts record shelf equalization for equalization setup EO1 through EO4.
SHLF	2 3	4		Jon	Called transport speed des

STEP 14 Adjust master bias control for selected equalization clockwise to reduce indicated output obtained in step 11 by amount shown for overbias in Table 5-9.

- STEP 15 Select INPUT/ALL, and increase oscillator level to give a 0-vu indication.
- STEP 16 Select REPRO/ALL. All channels should indicate 0 vu ±0.25 vu. If any channels do not fall within limits, readjust channel bias normalizing (paragraph 5-39) and repeat steps 4 through 15.
- 5-45 Record Equalization Adjustment (Method 1)
- STEP 1 Perform steps <u>1</u> through <u>16</u> of paragraph 5-44 procedure for checking bias normalizing and setting master bias.
- STEP 2 Select INPUT/ALL and adjust oscillator frequency to 1 kHz and a level to give 0-vu meter indication (at 7.5 in/s, press the +10-dB VU meter switch on the secondary control panel to permit a 0-vu indication for a 10-vu record level).
- STEP 3 Turn all in-use HF equalizers fully counterclockwise. (These are 20-turn potentiometers.)
- STEP 4 Select REPRO/ALL.
- STEP 5 Place machine in record mode, and adjust record gain for equalizer in use to give a 0-vu indication. (This is a preliminary adjustment only.)
- STEP 6 Increase oscillator frequency to 10 kHz (15 kHz for 30 in/s).
- STEP 7 Adjust in-use shelf equalizers (REC SHLF) to bring 10-kHz level (15 kHz at 30 in/s) to 0-vu indication.
- STEP 8 If the initial level in the preceding step was 2 dB more or less than 0 vu, reset oscillator frequency to 1 kHz and readjust record gain to 0 vu, then repeat preceding step.
- STEP 9 Set oscillator to system upper band edge frequency for the speed in use (15 kHz at 7.5 in/s, 20 kHz for 15 in/s, and 30 kHz for 30 in/s).
- STEP 10 Adjust all in-use HF equalizers for equalization in use to give an indication of -1.5 vu.
- STEP 11 Reset oscillator to 10 kHz (15 kHz at 30 in/s) and adjust shelf equalizers to bring level back to 0 vu.
- STEP 12 Recheck steps 9 through 11, since some interaction between shelf and HF equalizers exists.
- STEP 13 Set oscillator back to 1 kHz. Select INPUT/ALL and reset oscillator level to give a 0-vu meter indication.

NOTE: This procedure may result in some channels having HF SHECF fully CW, but response Ampex 4890425-01 low of 10 K. If so, adjust HF control for 0 W at 5-49 10 K (causes slight boost around 15 K). Both equalizers only active above 10 K. Add Note: This procedure is crazy. Works moderately well with 996 at 15 and 30, virtually useless with 456 at 15.

- STEP 14 Select REPRO/ALL and adjust all record gains for equalizer in use to give a 0-vu meter indication.
- STEP 15 Set oscillator to low-frequency band edge limit frequency (40 Hz at 30 in/s and 25 Hz at 15 and 7.5 in/s).
- STEP 16 Adjust appropriate reproduce low frequency equalizer for -1.5-vu meter indication. Note: Headburns at about (40 Hz, will be flat (0) at 50.
- STEP 17 Sweep frequency from low end limit to high end limit. Response should stay within limits shown in Table 5-10. Note: PB response exhibits slight dip around 4k.

## 5-46 Record Equalization Adjustment (Method 2)

- STEP 1 Perform procedure for checking bias normalizing and setting master bias (paragraph 5-44).
- STEP 2 Perform steps 2 through 12 of Method 1 record alignment (paragraph 5-45) for one channel only (preferably channel 1).
- STEP 3 Connect a 1-kHz square wave generator to all inputs (use of the audio test system will aid in this).
- STEP 4 Adjust generator level for a -3 to 0-vu indication on VU meters in INPUT monitoring. At 7.5 in/s reduce generator level to -10 vu and press +10 dB switch on secondary control panel. Place all channels in record. Select REPRO/ALL.
- STEP 5 Monitor channel prealigned in step 2 on one channel of a dual trace oscilloscope to display one or two cycles of reproduced square wave. Monitor other channels in turn on a second channel of oscilloscope.
- STEP 6 Adjust channel record gain if needed to ensure level does not exceed an indicated 0 vu.
- STEP 7 Adjust appropriate record HF and shelf equalizers for selected equalization to obtain an identical square wave on selected channel as a reference channel. Particular attention should be directed to pre- and post-shoot on leading and trailing edges. Figure 5-22 shows the effect of adjustment of record HF and shelf equalizers on the reproduced square wave. Note that any minor interaction effects can be readily seen.
- STEP 8 Repeat steps 6 and 7 as required for other channels.
- STEP 9 Reconnect the 1-kHz sine-wave generator. Select INPUT/ALL and adjust oscillator to give a 0-vu indication.
- STEP 10 Select REPRO/ALL and adjust record gain, for equalizers selected, to give a 0-vu output.

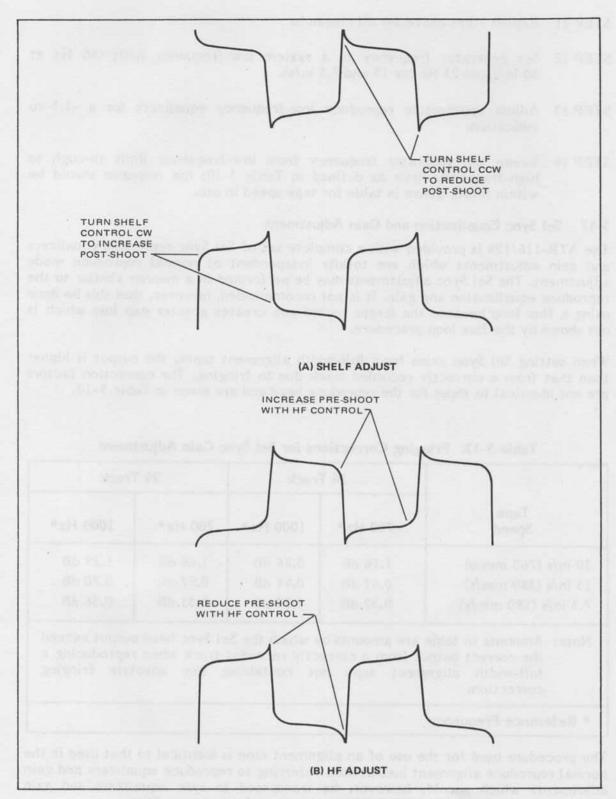


Figure 5-22. Square Wave Pre-Shoot and Post-Shoot

- STEP 11 Repeat steps above for all channels.
- STEP 12 Set generator frequency to a system low-frequency limit (40 Hz at 30 in/s and 25 Hz for 15 and 7.5 in/s).
- STEP 13 Adjust appropriate reproduce low-frequency equalizers for a -1.5-vu indication.
- STEP 14 Sweep the generator frequency from low-frequency limit through to high-frequency limit as defined in Table 5-10; the response should be within limits shown in table for tape speed in use.

## 5-47 Sel Sync Equalization and Gain Adjustment

The ATR-116/124 is provided with a complete set of Sel Sync reproduce equalizers and gain adjustments which are totally independent of normal reproduce mode adjustment. The Sel Sync adjustments may be performed in a manner similar to the reproduce equalization and gain. It is not recommended, however, that this be done using a flux loop because the larger record gap creates greater gap loss which is not shown by the flux loop procedure.

When setting Sel Sync gains from full-width alignment tapes, the output is higher than that from a correctly recorded track due to fringing. The correction factors are not identical to those for the reproduce head and are given in Table 5-12.

Table 5-12. Fringing Corrections for Sel Sync Gain Adjustment

	16 1	Track	24 Track		
Tape Speed	700 Hz*	10 <b>00</b> Hz*	700 Hz*	1000 Hz*	
30 in/s (760 mm/s)	1.16 dB	0.86 dB	1.66 dB	1.29 dB	
15 in/s (380 mm/s)	0.62 dB	0.44 dB	0.97 dB	0.70 dB	
7.5 in/s (190 mm/s)	0.32 dB	0.22 dB	0.51 dB	0.36 dB	

Note: Amounts in table are amounts by which the Sel Sync head output exceed the correct output from a correctly recorded track when reproducing a full-width alignment tape not containing any absolute fringing correction.

### \* Reference Frequency

The procedure used for the use of an alignment tape is identical to that used in the normal reproduce alignment instructions referring to reproduce equalizers and gain adjutments which should, however, be transposed to sync equalizers and gain adjustments. Note that SYNC LF EQ should be set from a recording.

The preferred method for adjusting Sel Sync equalization and gains is to reproduce, in the Sel Sync mode, a recording made on an aligned ATR-116/124 system; that is, record/repro gain and equalization must have been previously aligned.

### Make adjustments as follows:

- STEP 1 Connect audio oscillator to the line input or to the Audio Test PWA input.
- STEP 2 Set oscillator level for a 0-meter indication at 1 kHz in the Input monitor mode.
- STEP 3 Install tape of the type for which system record/reproduce equalization is aligned. Engage servos.
- STEP 4 Set system in record and select REPRO/ALL. At 7.5 in/s, select +10-dB meter sensitivity on secondary control panel to obtain a 0-vu indication.
- STEP 5 Record at 1 kHz for 1 minute (less time if only a few channels are being aligned).
- STEP 6 Rewind tape and place system in play mode with SYNC/ALL selected.
- STEP 7 Adjust the appropriate sync gain control (Table 5-13) for 0 vu.
- STEP 8 Place system in record with oscillator set to 10 kHz at 7.5 in/s, 15 kHz at 15 in/s, and 20 kHz at 30 in/s. These are the high-frequency limits.
- STEP 9 Record for 1 minute, then rewind and place system in play mode with SYNC/ALL selected.
- STEP 10 Adjust appropriate sync high-frequency equalizers to give a -1.5 vu indication.
- STEP 11 Place system in record with oscillator set to 45 Hz at 30 in/s and 30 Hz at 15 and 7.5 in/s. These are low-frequency limits.
- STEP 12 Record for 2 minutes, then rewind and place system in the play mode with SYNC/ALL selected.
- STEP 13 Adjust appropriate sync low-frequency equalizers to give a -1.5-vu indication.
- STEP 14 Repeat steps <u>8</u> through <u>13</u> with other spot frequencies as desired. The response of the sync channel should lie within the limits indicated in Table 5-14.

Table 5-13. Audio PWA, Handle Adjustments, Sync Equalization

	SYNC	۱, ۱	) _	Index No.	Name	Function
AVI	GAIN	3 4		1	SYNC GAIN	Adusts recorder/reproducer sel sync level for equalization setup EQ1 through EQ4.
ve	HF	3 4	2	2	SYNC HF	Adjusts high frequency sel sync equalization for equalization setup EQ1 through EQ4.
100	LF	1 2 3	3	3	SYNC LF	Adjusts low frequency sel sync equalization for equalization setup EQ1 through EQ4.
		) 4	)	1.40	100933 251	2014 . Set waters in month and a

Table 5-14. Frequency Response Limits for Sel Sync

Speed	Frequency Response At 1 kHz Reference		
30 in/s	45 Hz - 20 kHz	±2 dB	
15 in/s	30 Hz - 15 kHz	±2 dB	
7.5 in/s	30 Hz - 10 kHz	±2 dB	
	at 10 vu		

Note: 0 vu - 370 nWb/m with Ampex 456 tape.

## 5-48 Head Preamplifier Alignment

The reproduce and synce preamplifiers (Figure 5-23) consist of four PWAs (16-channel system) or six PWAs (24-channel system). Each PWA contains both Sel Sync and reproduce preamplifiers for four channels. The reproduce head preamplifier contains a high frequency head damping control, and the Sel Sync head preamplifier contains a low frequency compensating adjustment.

Readjustment of any preamplifier PWA should only be required following component replacement, head replacement, or use of a different head assembly. If this use is only temporary, the main reproduce and Sel Sync equalizers usually have sufficient range to achieve satisfactory response. However, optimum performance is obtained by appropriate realignment of the head preamplifier.

The adjustment procedure which follows should only be performed using a flux loop. Ampex Part No. 4020484 is recommended.

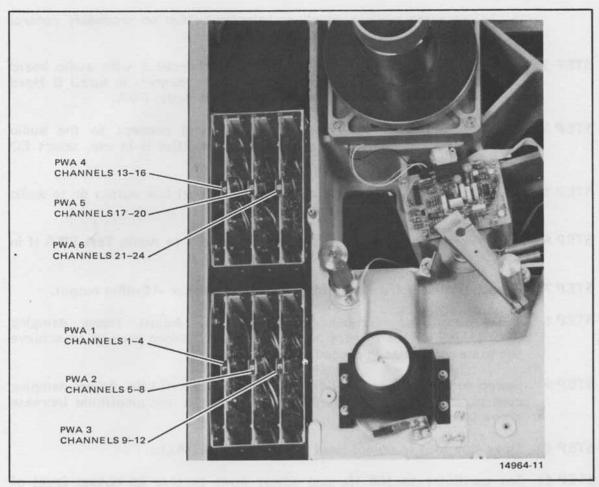


Figure 5-23. Pre-Amp PWA Location (Transport Trim Removed)

Use of the Head Preamplifier Test PWA, Ampex Part No. 4051078, removes the need to readjust an Audio PWA to perform the preamp alignment.

STEP 1 Remove top plate trim, locate Head Preamplifier PWA No. 1 (Figure 5-23), and remove and reinstall on an extender board.

#### Note

Preamplifier PWA No. 1 covers channels 1 through 4; Preamplifier PWA No. 2 covers channels 5 through 8, etc.

- STEP 2 Omit this step if Head Preamp Test PWA is being used; otherwise, proceed as follows:
  - a. On the Audio PWA, adjust one of the four reproduce and sync equalizers as follows:

Repro and sync hi — fully counterclockwise Repro and sync lo — fully clockwise

- b. Select same number equalizer selector button on secondary control panel as selected in sub step 2a.
- STEP 3 Temporarily replace Main Audio PWA in channel 1 with audio board adjusted in step 2. (This board is used for all channels in turn.) If Head Preamp Test PWA is in use, replace with Main Audio PWA.
- STEP 4 Place flux loop on the reproduce head and connect to the audio oscillator. (If Ampex flux loop equalizing amplifier is in use, select EO position marked 0.)
- STEP 5 Connect an ac voltmeter to appropriate channel line output or to audio test output.
- STEP 6 Apply system power. Select channel under test to Audio Test PWA if in use. Select REPRO/ALL.
- STEP 7 Adjust oscillator frequency for 1 kHz and level for -10-dBm output.
- STEP 8 Reset oscillator frequency to 25 kHz. Adjust repro damping R50/R51/R79/R108 (Figure 5-24) on channel 1 repro preamp to achieve the same reading as in preceding step.
- STEP 9 Sweep oscillator frequency from 1 kHz through 40 kHz. Adjust damping control, if needed, for widest response without any amplitude increase above level in step 7.
- STEP 10 Move flux loop to record head and select SYNC/ALL.
- STEP 11 Set oscillator to 100 Hz and adjust level to give an output level of -10 dBm.
- STEP 12 Change frequency to 1 kHz. Adjust channel 1 sync preamp low frequency boost control R13/R41/R69/R112 (Figure 5-24) on Preamp PWA for same reading as in step 11.
- STEP 13 Recheck level at 100 Hz and repeat preceding step if 100-Hz level is different from level set in step 11.
- STEP 14 Remove system power, replace Audio PWA in channel 1. Place specially adjusted Audio PWA or Head Preamp Test PWA in channel 2 and repeat steps 6 through 13.
- STEP 15 Repeat procedure as required for other channels.
- STEP 16 Replace Head Preamp PWA and top trim. Replace specially adjusted Audio PWA in original slot if Head Preamp Test PWA was not used.
- STEP 17 Readjust Audio PWA for correct response on repro and sync equalization position previously readjusted.

## 5-49 Record Head Matching Adjustment

The record head is connected to the record amplifier via a network which, at bias frequencies, transforms the complex impedance of the record head and cable into a resistive load. This network ensures maximum bias power transfer to the record head and consequently minimum dissipation in the record amplifier for a particular value of bias current.

Adjustment should only be required following component replacement, record head replacement, or head assembly change. Temporary change of head assembly does not necessitate the adjustment because sufficient margin in bias power is available. Optimum performance in record amplifier head-room results however, if the adjustment is performed.

STEP 1 Place Audio PWA to be adjusted on an extender board and reinstall.

STEP 2 Connect oscilloscope to display signal at TP302 (channel 1) and signal at pin 7 (channel 2) relative to TPG.

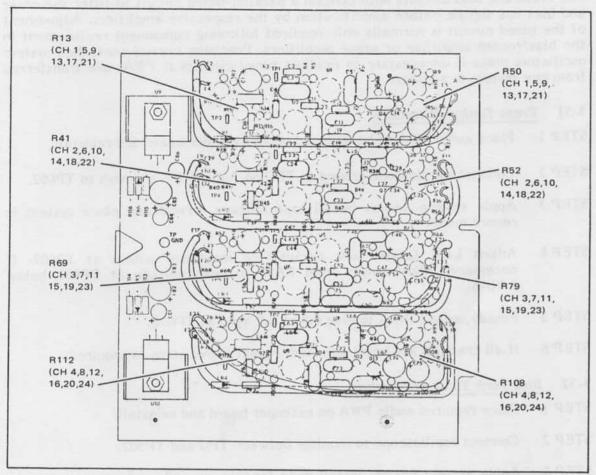


Figure 5-24. Audio Preamplifier, Equalization Preamplifier Control

- STEP 3 Apply system power and place system in record mode. Remove any audio signal at system input.
- STEP 4 Adjust time base so that one cycle is equal to four horizontal divisions (90° per division). Center both traces by temporarily removing them and adjusting vertical position controls.
- STEP 5 Adjust head matching L303 for a display which indicates a 90° phase shift between the two traces. This will occur when zero crossings of two traces are one division apart.
- STEP 6 Remove system power and repeat above steps for other channels.
- STEP 7 Perform bias normalizing procedures for any and all channels which have been adjusted.

## 5-50 Erase and Bias Tuned Circuit Adjustment

The erase and bias circuits both contain a parallel-tuned circuit to filter the erase and bias bus signals before amplification by the respective amplifiers. Adjustment of the tuned circuit is normally only required following component replacement in the bias/record amplifier or erase amplifiers. Precision crystal-controlled system oscillators make it unnecessary to readjust tuned circuits if PWAs are transferred from one system to another.

## 5-51 Erase Tuning Procedure

- STEP 1 Place audio PWA to be adjusted on an extender board and reinstall.
- STEP 2 Connect oscilloscope ground to TPG on Audio PWA and high to TP602.
- STEP 3 Apply system power, install tape (engage servos) and place system in record mode.
- STEP 4 Adjust L601 (erase tank circuit) for maximum output at TP602. If necessary, adjust erase level R616 to keep voltage at TP602 below 1 Vp-p.
- STEP 5 Finally, adjust R616 to give 0.8 to 0.9 Vp-p at TP602.
- STEP 6 If all channels are being adjusted, repeat above steps as required.

## 5-52 Bias Tank Tuning Procedure

- STEP 1 Place required audio PWA on extender board and reinstall.
- STEP 2 Connect oscilloscope to monitor between TPG and TP302.
- STEP 3 Apply system power, install tape (engage servos), and place system in record mode.

- STEP 4 Adjust bias tank inductor L301 for maximum output at TP302.
- STEP 5 Repeat steps 1 through 4 as needed for other channels.
- STEP 6 Perform bias normalizing procedures for all channels which have been adjusted.

## 5-53 Common Mode Rejection

Adjustment of the Audio PWA for common mode rejection involves setting level balance and input level and gain/phase balance of the input amplifier section of the Audio PWA. Normally this adjustment will be required only following component change to the line input amplifier section.

- 5-54 Level Balance. To adjust level balance, proceed as follows:
- STEP 1 Select Audio PWA corresponding to channel being adjusted.
- STEP 2 Place PWA for channel being adjusted on an extender PWA.
- STEP 3 Connect a grounding jumper from PWA metal backplane to chassis of cage.

### CAUTION

TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS ON A PWA ALWAYS TURN RECORDER/REPRODUCER POWER OFF BEFORE INSTALLING OR REMOVING THE PWA.

- STEP 4 Perform a rough adjustment of input level control as follows:
  - a. Set signal generator to provide sinewave input at desired studio line level, e.g., +4 dBm at 1 kHz.

#### Note

Signal generator should be connected to the input using normal configuration; do not short line hi and line lo for this adjustment.

- Select INPUT monitoring on that channel.
- c. Adjust input level control R513 (Figure 5-25 or 5-26) for 0 vu on the machine VU meters.
- STEP 5 Short line hi and line lo inputs together for channel being adjusted. Note: A plug can be made up for this test procedure (see Figure 5-26).
- STEP 6 Connect a sinewave signal generator between ground and the shorted input terminals. Set generator level to about 5 Vrms (16 dBm).
- STEP 7 Select the input monitor mode and look at the output with a voltmeter or oscilloscope connected to TP501 (Figure 5-25 or 5-26).

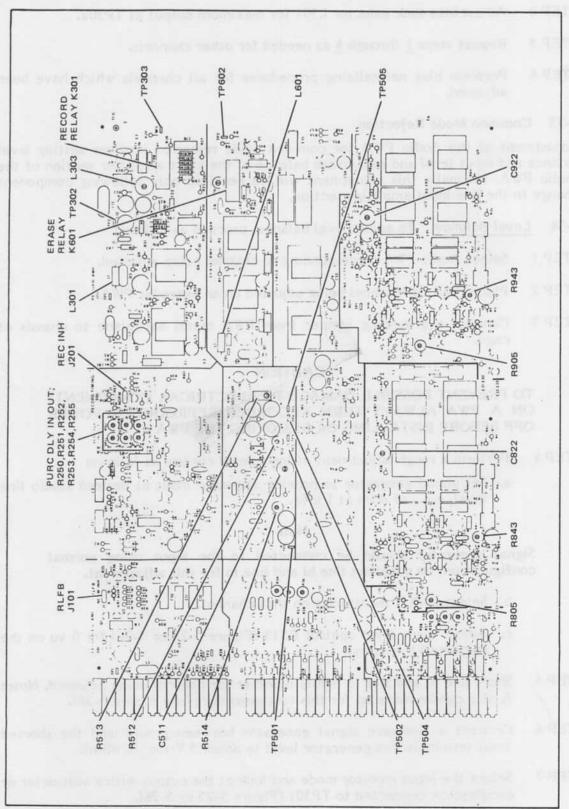


Figure 5-25. Audio PWA Assembly No. 4050989 Adjustments, Jumpers, and Test Points

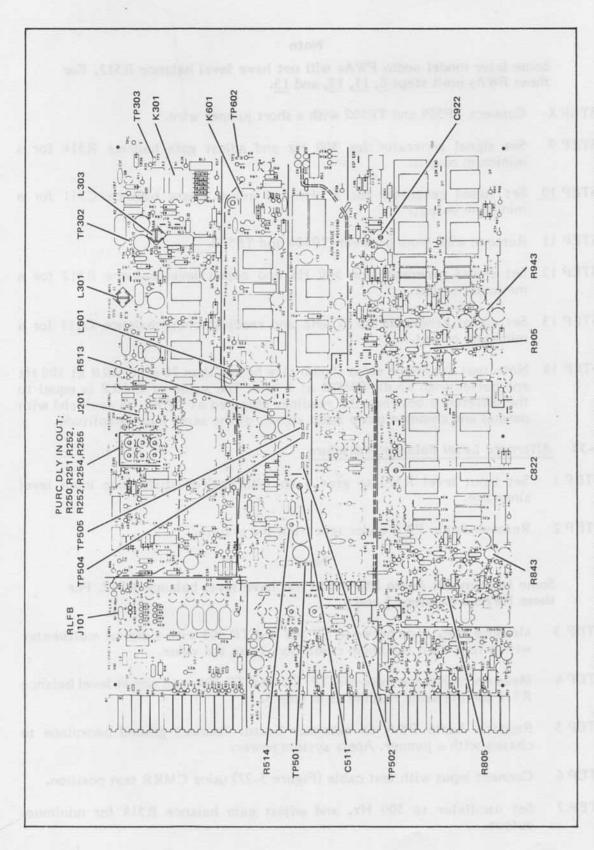


Figure 5-26. Audio PWA Assembly No. 4051080 Adjustments, Jumpers, and Test Points

### Note

# Some later model audio PWAs will not have level balance R512. For these PWAs omit steps 8, 11, 12, and 13.

- STEP 8 Connect TP504 and TP502 with a short jumper wire.
- STEP 9 Set signal generator for 500 Hz and adjust gain balance R514 for a minimum output.
- STEP 10 Set signal generator for 5 kHz and adjust phase balance C511 for a minimum output.
- STEP 11 Remove wire from between TP504 and TP502.
- STEP 12 Set signal generator for 500 Hz and adjust level balance R512 for a minimum output.
- STEP 13 Set signal generator for 5 kHz and readjust phase balance C511 for a minimum output.
- STEP 14 Note that the above steps should give better than 70 dB CMRR at 500 Hz and better than 65 dB CMRR at 5 kHz. The value of CMRR is equal to the difference between the readings obtained at TP501 (in decibels) with normal and common mode input signals of the same input amplitude.

## 5-55 Alternate Level Balance Procedure

- STEP 1 Set input level R513 to give 0 vu with desired studio line input level sinewave.
- STEP 2 Remove Audio PWA under test from the system.

### Note

# Some later model Audio PWAs will not have level balance R512. For these PWAs omit steps 3 and 4.

- STEP 3 Measure resistance between TP 502 and TP 503 with a digital multimeter with a four-digit minimum resolution. Note the value.
- STEP 4 Measure resistance between TP 505 and TP 504, and adjust level balance R512 for the same reading as in step 3.
- STEP 5 Replace Audio PWA on extender board. Connect ground backplane to chassis with a jumper. Apply system power.
- STEP 6 Connect input with test cable (Figure 5-27) using CMRR test position.
- STEP 7 Set oscillator to 500 Hz, and adjust gain balance R514 for minimum output.

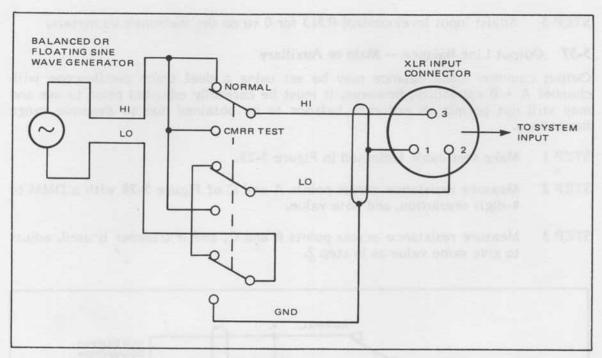


Figure 5-27. Test Lead/Switch for Measuring/Adjusting Input CMRR

- STEP 8 Set oscillator to 5 kHz, and adjust phase balance C511 for minimum output.
- STEP 9 Reapply normal line input and adjust input level R513 as needed for a 0-vu meter indication.
- STEP 10 Note that the result of the above should give better than 70 dB CMRR at 500 Hz and better than 65 dB CMRR at 5 kHz. The value of CMRR is equal to the difference between readings obtained at TP501 (in dB) with normal and common mode input signals of the same value.
- 5-56 Input Level. To adjust input level proceed as follows:
- STEP 1 Check VU meter mechanical zero with power off.
- STEP 2 Perform level balance, paragraph 5-54.
- STEP 3 Select INPUT monitoring for channel being adjusted.
- STEP 4 Set signal generator to provide a sinewave input at the desired studio line level, e.g., +4 dBm at 1 kHz.

### Note

Signal generator should be connected to the input using normal configuration; DO NOT short line hi and line lo for this adjustment.

STEP 5 Adjust input level control R513 for 0 vu on the machine's vu meters.

### 5-57 Output Line Balance - Main or Auxiliary

Output common mode balance may be set using a dual trace oscilloscope with channel A + B capability; however, it must be carefully adjusted prior to use and may still not permit an accurate balance to be obtained due to dynamic range limitations.

- STEP 1 Make test cable indicated in Figure 5-28.
- STEP 2 Measure resistance across points A and C of Figure 5-28 with a DMM of 4-digit resolution, and note value.
- STEP 3 Measure resistance across points B and C, and if trimmer is used, adjust to give same value as in step 2.

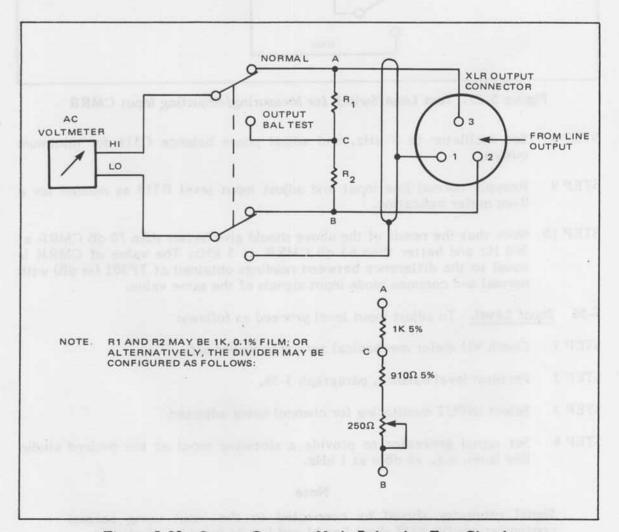


Figure 5-28. Output Common Mode Balancing Test Circuit

- STEP 4 Place Audio PWA to be adjusted on extender board. Attach grounding jumper between Audio PWA backplane and card cage.
- STEP 5 Apply system power and select INPUT monitoring.
- STEP 6 Connect a sinewave signal generator to line input. Set generator frequency to 500 Hz and generator level to 5 Vrms (about +16 dBm).
- STEP 7 Monitor line output (main or auxiliary as appropriate) with test cable of steps 1-3 using output balance test position.
- STEP 8 Adjust gain balance R943 (R843 auxiliary) for a minimum output.
- STEP 9 Change generator frequency to 5 kHz.
- STEP 10 Adjust phase balance C922 (C822 auxiliary) for a minimum output.
- STEP 11 Repeat steps 8 and 10 as necessary, as there is a slight interaction.
- STEP 12 Note that output CMRR should be better than 45 dB at 500 Hz and better than 40 dB at 5 kHz.

### 5-58 Output Level

To adjust line or auxiliary output level, proceed as follows:

- STEP 1 Apply input signal of 1 kHz from a sinewave generator.
- STEP 2 If machine is to operate into a 600- $\Omega$  load, connect a 600- $\Omega$  resistor between pins 2 and 3 of the output connector.
- STEP 3 Select input monitor mode.
- STEP 4 Adjust input signal level until VU meters indicate 0 vu.
- STEP 5 Connect ac voltmeter to line output of the channel selected.
- STEP 6 Adjust R905 (R805 auxiliary) for line output level desired.

#### Note

The 0 vu line output level will normally be the same as the 0 vu line input level. The systems are factory set for +4.0 dBm line input and line output.

## 5-59 Erasure Depth Adjustment and Measurement

Erase current supplied to the erase head is adjustable by means of master erase bus potentiometer control R8 on the VSO PWA and by an individual erase current trimmer on each Audio PWA. The erase current is the only adjustment required for

the erase system. Because of the extreme erase depth of which the recorder/reproducer is capable, it is mandatory that tape used for adjustment and depth measurement be thoroughly bulk-degaussed. This prevents any crosstalk from an unerased portion of the tape being interpreted as the erased signal level. For accurate measurement of erasure depth, a spectrum analyzer, wave analyzer, or 1/10 octave filter should be used. If these instruments are unavailable, a reasonably accurate adjustment can be made by listening to the erased signal at an elevated monitoring level. The erase performance specifications given in this procedure apply to Ampex 406, 407, or 456 tape or the exact equivalent. Proceed as follows:

- STEP 1 Clean and demagnetize heads and other tape path components as described in paragraph 5-3.
- STEP 2 Install VSO PWA on extender board.
- STEP 3 Set master erase bus level control R8 on the VSO PWA to give 6 Vp-p at Audio PWA pin 26 on the PWA edge connector.
- STEP 4 If Audio Test PWA is used, connect a spectrum analyzer, wave analyzer, or 1/10 octave filter to appropriate output connector, and connect an audio oscillator to appropriate input connector.
- STEP 5 If Audio Test PWA is not used, connect a spectrum analyzer, wave analyzer, or 1/10 octave filter to appropriate recorder/reproducer output connector and connect an audio oscillator to appropriate 1/0 panel input connector.
- STEP 6 Apply power, thread a reel of bulk-degaussed tape of same kind that was used to align the reproduce and record circuits, and engage servos.
- STEP 7 Set speed-select switch to highest operating speed.
- STEP 8 Place system in record mode (channels not under test should also be placed in record mode).
- STEP 9 Set oscillator frequency to appropriate frequency as follows: 1 kHz at 30 in/s, 500 Hz at 15 in/s, or 250 Hz at 7.5 in/s. Adjust oscillator output level for +6 dBm at output of Audio Test PWA or +10 dBm at machine output connector.
- STEP 10 Adjust analyzer to zero reference, or note analyzer range setting and meter reading.
- STEP 11 Reset tape timer display to zero.
- STEP 12 Record continuously for 5 minutes and rewind tape to tape timer display zero.
- STEP 13 Remove oscillator and short signal input terminals (or short input with an impedance not greater than 300  $\Omega$ ).

- STEP 14 Again place system into record mode and adjust analyzer range setting to observe residual erase signal level.
- STEP 15 Adjust channel erase control R616 on Audio PWA slowly counterclockwise, and note when erased signal's amplitude suddenly increases. Then adjust erase control slowly clockwise until erase signal is 85 dB below unerased level established in step 8 (-79 dBm at output of Audio Test PWA, or -75 dBm at machine output connector). If a wave analyzer or spectrum analyzer with a resolution bandwidth less than 5 Hz is being used, continue turning erase control clockwise until a minimum amplitude erased signal is seen. Monitor level between TP602 and TPG. The level should be between 0.8 and 1.0 Vp-p.
- STEP 16 Repeat steps 13 through 15 for other channels.

### 5-60 PURC Timing Alignment

The recorder/reproducer is capable of operating with or without PURC operation. Adjustments required for PURC alignment are those for record/bias entry and exit delay timing to establish correct operation for each speed.

To aid in alignment of PURC timing, an optional automatic record/play cycler may be used to cycle recorder/reproducer for insert-edit operation while PURC timing adjustment is being made. (The cycler is constructed by the user. See Figure 5-29 for cycler schematic diagram and components.) The PURC alignment procedure should only be performed if record, reproduce, and erase alignments are known to be correct. Proceed as follows:

- STEP 1 Clean and demagnetize heads and other tape path components as described in paragraph 5-3.
- STEP 2 Connect an audio oscillator to audio input connector corresponding to first channel to be aligned.
- STEP 3 Set oscillator frequency to 1.0 kHz.
- STEP 4 Connect one channel of a scope to audio output connector corresponding to first channel to be aligned.
- STEP 5 Place Audio PWA for channel to be adjusted on an extender board.
- STEP 6 Connect second scope channel to U201-7 (TP201) and trigger from this.
- STEP 7 Apply power and thread a reel of tape on transport and engage servos.
- STEP 8 Place all channels into record mode. Select 30-in/s transport speed. There are PURC adjustment controls for each speed.
- STEP 9 Adjust oscillator output level for system operating level; 0 dBm at output of Audio Test PWA or +4 dBm at machine output connector.

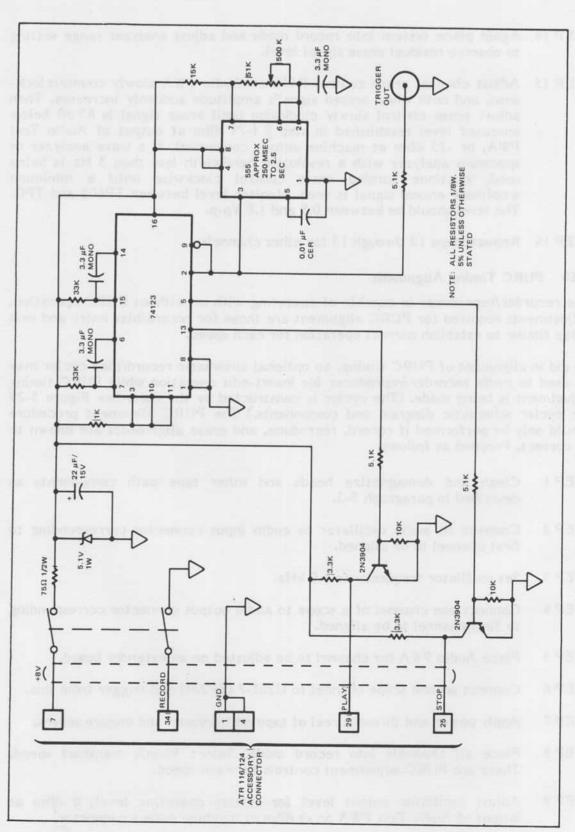


Figure 5-29. PURC Automatic Record/Play Cycler

- STEP 10 Set tape timer display to zero and record continuously for 5 minutes.
- STEP 11 Rewind tape to tape-timer zero.
- STEP 12 If automatic cycler is being used, connect cycler to the external remote control connector (Figure 2-3) and trigger scope from U201, pin 7 (TP201) from the positive-going edge for ingoing and negative-going edge for outgoing.
- STEP 13 Change oscillator frequency to 1.5 kHz.
- STEP 14 Reapply power and place system into play mode with channel being adjusted in ready mode and other channels in safe mode.
- STEP 15 If cycler is used, turn power on and adjust cycle rate time control R1 on to show ingoing and outgoing edges of insert on scope. Adjust PURC timing control R251 on Audio PWA (Figure 5-25 or 5-26) to minimize overlap on ingoing insert and R250 to minimize gap on outgoing edge, as viewed on scope. Alternately adjust scope delayed triggering with 20 ms/cm. Delay sweep to view either ingoing or outgoing edit point. The delay from the trigger to waveform is about 140 ms at 30 in/s, 240 ms at 15 in/s, and 440 ms at 7.5 in/s.
- STEP 16 If cycler is not being used, hold RECORD depressed and alternately depress PLAY and STOP. This places the system in and out of record mode without stopping the system. Adjust R251 and R250 for condition described in step 15. Repeat pressing of PLAY and adjust R251 and R250 as required to achieve conditions described in step 15.
- STEP 17 Change transport speed to 15 in/s and perform several insert edits (step 15 or 16), adjust R253 and R252 (R255 and R254 for 7.5 in/s).
- STEP 18 Repeat steps 2 through 17 for other channel(s) selected for PURC operation, and for other tape speed.
- STEP 19 Remove power and remove extender board from electronics assembly.

  Reinstall Audio PWA into electronics assembly.
- STEP 20 If automatic cycler was used, disconnect cycler from ATR-116/124.
- STEP 21 Disconnect audio oscillator from audio input connector.

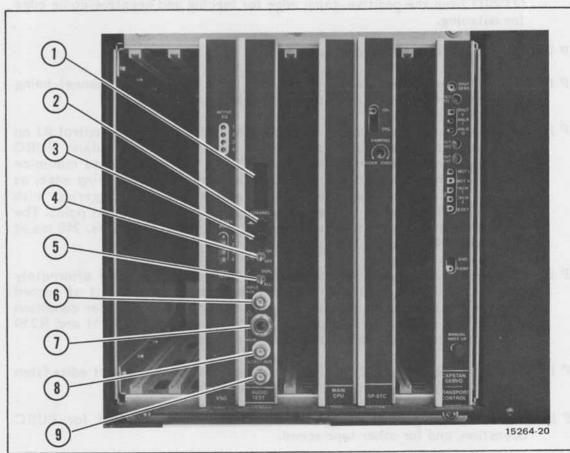
#### 5-61 Audio Test PWA

Table 5-15 summarizes operation of the Audio Test PWA. The ATR-116/124 provides front panel access to signal system input and output via the Audio Test PWA. A signal generator can be connected to the input of any audio channel (as selected by the INC or DEC pushbutton switch and displayed by the two-digit LED display) or to all inputs simultaneously. A voltmeter or oscilloscope can be connected to the output of any channel.

### Note

The operating level (0 vu) on the input and output of the Audio Test PWA always corresponds to 0 dBm.

Table 5-15, Audio Test PWA, Controls/Connectors/Indicators



Index No.	Name	Function
1	Channel display	Display indicates channel accessed at Audio Test PWA handle connectors.
2	▲Increment	Increments channel accessed at Audio Test PWA handle connectors.
3	▼Decrement	Decrements channel accessed at Audio Test PWA handle connectors.
4	ON/OFF switch	Connects/disconnects Audio Test PWA from I/O bus system.

Table 5-15, Audio Test PWA, Controls/Connectors/Indicators (Continued)

Index No.	Name	Function
5	CH DSPL/ALL bus selector	In DSPL position only the channel displayed is fed an input signal. In ALL positions, all channels are fed an input signal (signal generator input to Audio Test PWA handle is routed to all channels).
6	Input bus connector	Accepts signal generator input to input bus.
7	MAIN headphone connector	Headphones connector, accepts standard 1/4-in. phone plug, allows operator to monitor channel indicated on display with headphones.
8	Main output bus connector	Output of line amplifier, accepts VTVM or oscilloscope for monitoring main channel indicated on display.
9	Aux output bus connector	Output of auxiliary amplifier, accepts VTVM or oscilloscope for monitoring auxiliary channel indicated on display.
street, start	a produced velocity	Note
University of the second	received and the second and the seco	The performance of the audio test signal system is not identical in some respects to the input-output performance obtained from the machine's individual input and output connectors. In almost all cases, however, these differences are negligible when measuring off-tape performance.
0414	the tape. For 2.5 infa-	

### 5-62 PERFORMANCE TESTS

Use the following performance test procedures to check tape tension, speed variation, operating level, signal-to-noise ratio, harmonic distortion, interdemodulation distortion, and flutter. The performance test should be performed after each 500 hours of operation to ensure the recorder/reproducer is performing in accordance with specifications given in Table 1-4. Also, an applicable performance test should be performed whenever equipment appears to be malfunctioning, and after making repairs to the equipment that could affect performance.

Test equipment required for the performance tests is listed in Table 5-1. In the event a performance test is unsatisfactory, refer to troubleshooting section of the manual and perform the appropriate alignment, adjustment, or corrective maintenance procedure.

## 5-63 Tape Tension

If tape should creep in either direction while in stop mode, or tape tension appears to be incorrect, check tape tension as follows:

- STEP 1 Thread tape on recorder/reproducer with approximately even tape pack on both reels.
- STEP 2 Turn power on and engage servos.
- STEP 3 Measure tape tension by engaging tentelometer between reel and the first tape guide as in Figure 5-11 and on both supply and takeup sides. Tension should be 9 ± 0.5 oz.
- STEP 4 Manually spin capstan edit knob in one direction and then in the opposite direction with equal force. Tape should coast an equal amount in each direction.
- STEP 5 Turn on recorder, engage servos, and put in play mode, then check capstan current by checking voltage across the MOT 1 and GND jacks of Capstan Servo PWA. Voltmeter reading should be between -200 and -600 mV.

## 5-64 Operating Level

To determine or check the operating level of the recorder/reproducer, play back a standard alignment tape. (Refer to paragraph 5-25 and paragraph 5-28.)

The following procedures can be used to determine recorder/reproducer operating levels of 370 nWb/m, or 185 nWb/m with the use of 185-nWb/m reference level alignment tape.

#### Note

On Ampex alignment tapes for 15 and 30 in/s, the 185-n/Wb/m, 700-Hz reference tone is the first tone on the tape. For 7.5 in/s, the 185-nWb/m, 700-Hz tone is the last tone on the tape.

To check operating level, proceed as follows:

- STEP 1 Clean and demagnetize heads and other tape path components as described in paragraph 5-3.
- STEP 2 Select system tape speed at setup panel and appropriate equalization on secondary control panel.
- STEP 3 If the Audio Test PWA is not being used, connect an ac voltmeter to appropriate recorder/reproducer output connector (Figure 2-3).
- STEP 4 Reproduce the 185-nWb/m operating level 700-Hz tone for 7.5, 15, or 30 in/s of an Ampex standard alignment tape.

STEP 5 If an ac voltmeter is being used at output of recorder/reproducer, the operating level can be determined from the ac voltmeter reading as follows:

- Inequestica	VU Meter	Machine Line Out	Audio Test PWA
370 nWb/m	-6	-2 dBm	-6 dBm
260 nWb/m	-3	+1 dBm	-3 dBm
185 nWb/m	0	+4 dBm	0 dBm

For the above, add correction factors of Table 5-5 if a full width alignment tape is used.

#### Note

Step 5 assumes that the ATR-116/124 has been calibrated for a line output operating level of +4 dBm (0 vu on VU meter).

### 5-65 Signal-to-Noise Ratio

Signal-to-noise measurement is made using a filter connected to the output of the system to attenuate noise out of the audible-frequency band. Figure 5-30 is a simple passive filter for passing frequencies in the 30-Hz to 18-kHz frequency band and Figure 5-31 is a filter for weighting to the ANSI A characteristic. To use the ANSI A filter shown in Figure 5-31, it is necessary to correct for a 4 dB insertion loss of the filter, that is, +4 dB is added to the ac voltmeter indication when making the measurement. For example, if the meter reads -61 dBm through the filter, the actual reading is -57 dBm.

Figure 5-32 is a schematic diagram of a universal noise filter (constructed by the user) that has a four-position selector switch for measurement to standards CCIR, ANSI A weighted, and 30 Hz -18 kHz. The fourth position of the selector switch enables the filter to be used as a buffer. A gain switch permits unity gain or 20 dB gain.

Table 5-16 gives signal-to-noise ratios for tape speed, equalization standard, track format, and noise measurement weighting filter in use when using Ampex 456 tape (or direct equivalent), and with the recorder adjusted for 370 nWb/m operating level at 700 Hz. Table 5-18 provides typical signal-to-noise ratios with the system in standby mode. All signal-to-noise ratios given in Tables 5-16 and 5-17 are measured relative to nominal 3% third harmonic distortion which is 9 dB above 370 nWb/m level when using Ampex 456 tape. Signal-to-noise ratio measurement should only be performed if the reproduce, record, and erase system alignments have been performed or are known to be correct. Also, signal-to-noise ratio measurements should be made at the recorder I/O panel only.

To measure signal-to-noise ratio, proceed as follows:

STEP I Clean and demagnetize heads and other tape path components as described in paragraph 5-3.

- STEP 2 Apply power, thread a reel of bulk-degaussed tape on the transport, and engage servos.
- STEP 3 Set speed switch to tape speed selected for measurement.
- STEP 4 Place system in record mode (channels not under test should also be placed in record mode).
- STEP 5 Connect oscillator to the I/O panel input connector of the desired channel and an ac voltmeter at the output connector. Set oscillator frequency to 1.0 kHz, and adjust oscillator output level for +9 dB above an operating level of 370 nWb/m (+13 dBm at the I/O panel output connector).

#### Note

Step  $\underline{5}$  assumes that the ATR-116/124 has been calibrated for a line output operating level of +4 dBm (0 vu on meter).

- STEP 6 Insert appropriate audio noise-band attenuation filter (CCIR, ANSI A weighted, or 30-Hz -18-kHz band limiting) between the output connector and ac voltmeter.
- STEP 7 Reset tape timer display to zero.

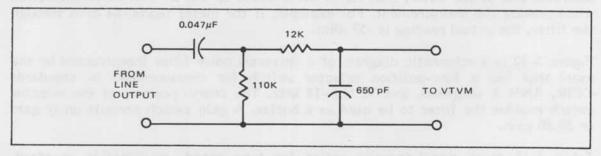


Figure 5-30. 30-Hz to 18-kHz Band Limiting Filter

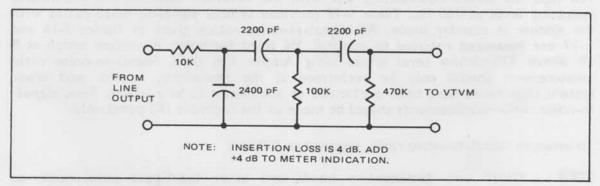


Figure 5-31. ANSI "A" Weighted Filter

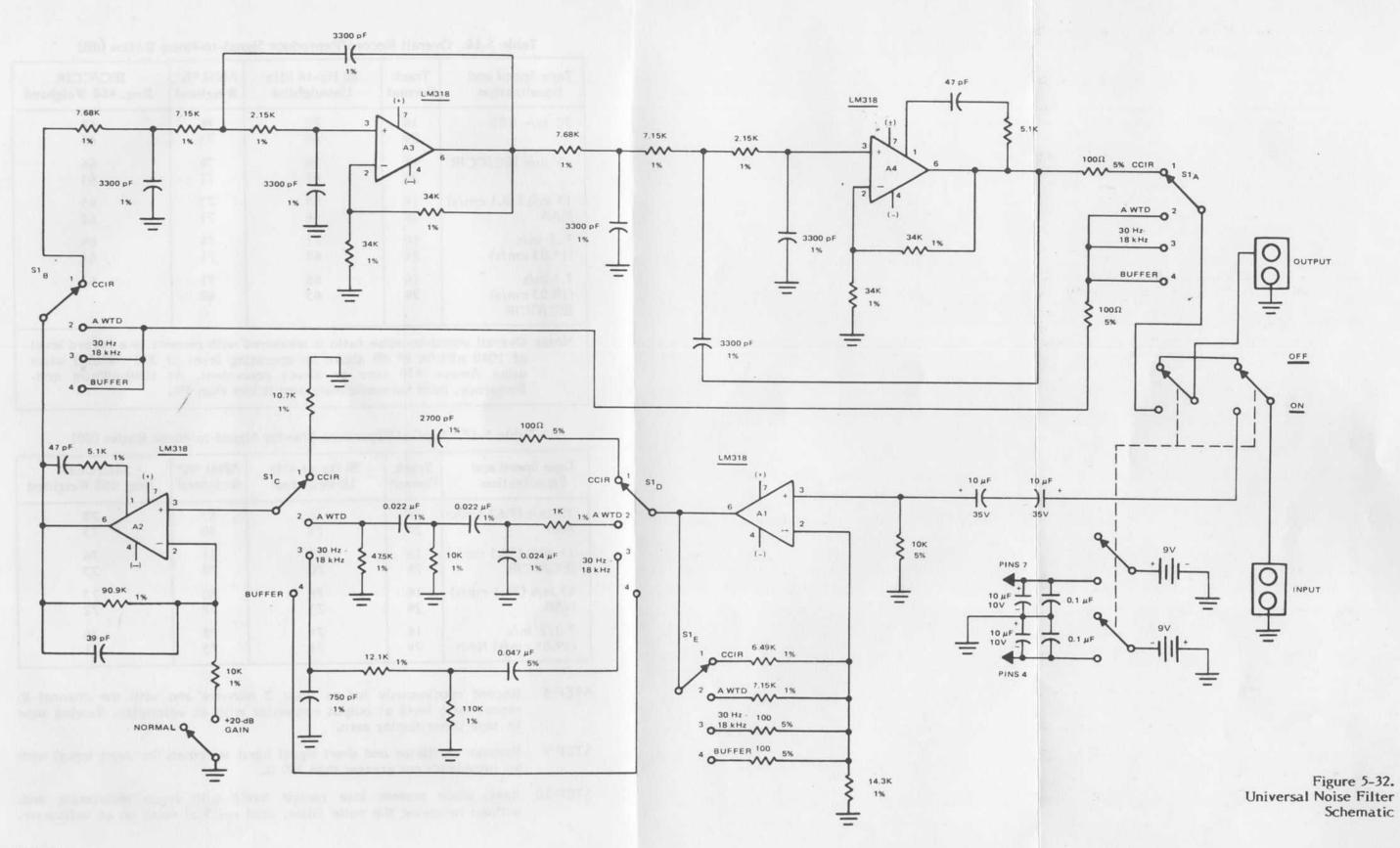


Table 5-16. Overall Record/Reproduce Signal-to-Noise Ratios (dB)

Tape Speed and	Track	30 Hz-18 kHz	ANSI "A"	IEC/CCIR
Equalization	Format	Unweighted	Weighted	Reg. 468 Weighted
30 in/s AES	16	72	76	68
	24	69	73	65
15 in/s IEC/CCIR	16	70	74	66
	24	67	71	63
15 in/s (38.1 cm/s)	16	69	73	65
NAB	24	66	71	62
7.5 in/s	16	71	74	64
(19.05 cm/s)	24	68	71	61
7.5 in/s (19.05 cm/s) IEC/CCIR	16 24	68 65	71 68	63

Note: Overall signal-to-noise ratio is measured with respect to a record level of 1040 nWb/m (9 dB above an operating level of 370 nWb/m) when using Ampex 456 tape or direct equivalent. At 1040-nWb/m mid-frequency, third harmonic distortion is less than 3%.

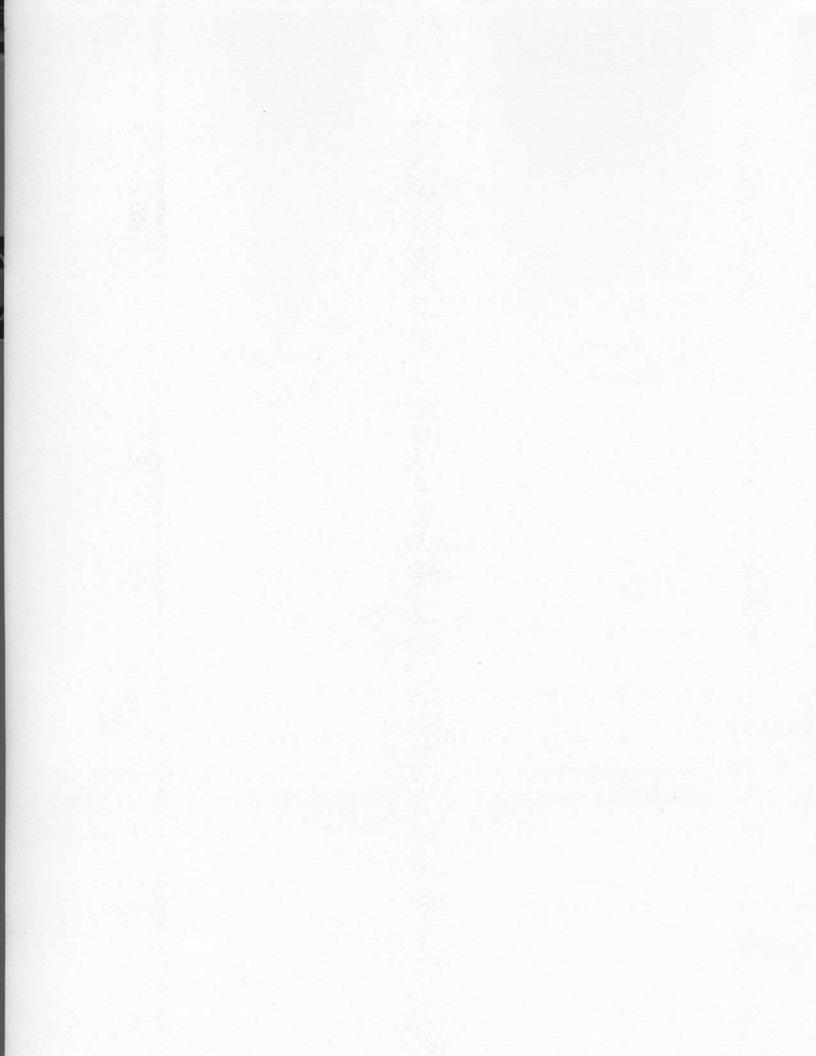
Table 5-17. Typical Reproduce Standby Signal-to-Noise Ratios (dB)

Tape Speed and	Track	30 Hz-18 kHz	ANSI "A"	IEC/CCIR
Equalization	Format	Unweighted	Weighted	Reg. 468 Weighted
30 in/s (7.62 cm/s)	16	76	83	78
AES	24	73	80	75
15 in/s (38.1 cm/s) IEC/CCIR	16	73	81	76
	24	70	78	73
15 in/s (38.1 cm/s)	16	76	80	75
NAB	24	73	77	72
7-1/2 in/s	16	74	78	74
(19.05 cm/s) NAB	24	71	75	71

STEP 8 Record continuously for at least 2 minutes and with the channel in repro, note level at output connector with ac voltmeter. Rewind tape to tape timer display zero.

STEP 9 Remove oscillator and short signal input terminals (or short input) with an impedance not greater than 300  $\Omega$ .

STEP 10 Again place system into record mode with repro monitoring and, without removing the noise filter, read residual noise on ac voltmeter.



Signal-to-noise ratio is difference between the reading in dB in this step and that of step  $\underline{8}$  and should exceed the associated overall figure in Table 5-16.

- STEP 11 Press STOP to stop transport and to place system into standby mode.
- STEP 12 Read residual noise on ac voltmeter without removing filter. The standby signal-to-noise ratio is the difference between the reading in dB in this step and that of step 8 and should be approximately equal to the associated value in Table 5-17.
- STEP 13 Repeat the procedure (steps 4 through 12) except in steps 8 and 10, record only and after rewinding to zero, monitor the sync output with the recorder in play. CCIR and ANSI A weighted values should be within ±3 dB of the repro values.

### 5-66 Harmonic Distortion

Harmonic distortion levels should be measured using a wave or spectrum analyzer. A total harmonic distortion analyzer should not be used. The audio oscillator used for measurement should not have a residual second harmonic component greater than 0.03% rms (-70 dB) for fundamental frequencies from 500 Hz to 1.0 kHz. Also the third harmonic component of the oscillator should not be greater than 0.05% rms (-66 dB). Values given are applicable only to the use of Ampex 456 tape, biased as shown in Table 5-9 and using a 370 nWb/m operating level. Typical values for third harmonic distortion for other types of tape will normally be in the range of 0.3% to 0.5% at recorded levels of 14 dB to 15 dB below midband saturation.

Table 5-18 gives harmonic and intermodulation distortion system specifications when Ampex 456 tape or its direct equivalent is used. The harmonic distortion measurement should only be performed if the reproduce, record, and bias adjustments have been correctly made or are known to be correct. Proceed as follows:

- STEP I Clean and demagnetize heads and other tape path components as described in paragraph 5-3.
- STEP 2 If Audio Test PWA is used, connect a spectrum analyzer or wave analyzer to appropriate handle output connector, and connect audio oscillator to appropriate handle input connector (Table 5-15).
- STEP 3 If Audio Test PWA is not used, connect spectrum analyzer or wave analyzer to appropriate recorder/reproducer output connector and connect audio oscillator to appropriate I/O panel input connector. Set frequency to 1 kHz.
- STEP 4 Apply power, thread reel of tape on transport and engage servos.
- STEP 5 Set speed switch to tape speed selected for measurement.
- STEP 6 Place system into record mode.

Table 5-18. Distortion Levels

Distortion	Туре	Recorded Flux Level	Distortion %
Even order of Third harmonic		370 nWb/m 370 nWb/m (0 vu) 1040 nWb/m (+9 vu)	<0.1% <0.3% <3.0%
SMPTE Interm	odulation	740 nWb/m (+6 vu) for IEC/AES equalizations 740 nWb/m (+6 vu) for NAB equalizations	<3% <4%

Note: The above figures are applicable only to Ampex 456 tape, biased as recommended in Table 5-9.

- STEP 7 Set oscillator frequency to 1 kHz and adjust oscillator output level for +4 dBm (0 vu) at the machine output connector.
- STEP 8 Adjust wave analyzer to measure second harmonic content; this should not exceed -60 dB with respect to level of fundamental set in step 7.
- STEP 9 Adjust wave analyzer to measure third harmonic content. This should not exceed -50 dB relative to level of fundamental set in step 7.
- STEP 10 Increase oscillator output level to system peak operating level. This is +13 dBm (+9 vu) at machine output connector, or +9 dBm at Audio Test PWA output.
- STEP 11 Adjust wave analyzer to measure third harmonic content. This should not exceed -30 dB relative to level of fundamental set in step 10.
- STEP 12 Repeat entire procedure for each channel.

## 5-67 SMPTE Intermodulation Distribution

Intermodulation distortion is produced by nonlinearity in the record/reproduce process. This produces frequencies in the output signal equal to the sums and differences of integral multiples of the component frequencies present in the input signal (harmonics not included). Measurement of intermodulation distortion is a convenient method of obtaining a qualitative indication of system performance. However, a reading in excess of specifications gives no indication of the possible cause, as a poor or damaged tape may produce amplitude fluctuations in high-frequency carrier which greatly exceed the true intermodulation products. Therefore, judgment is required when attempting to interpret the measurements.

Table 5-18 gives harmonic and intermodulation distortion system specifications when Ampex 456 tape equivalent is used. The measurement should only be

performed if reproduce, record, and bias adjustments have been performed or are known to be correct. To measure intermodulation distortion as defined by the SMPTE, execute steps  $\underline{1}$  through  $\underline{6}$  of paragraph 5-66 above and proceed as follows:

- STEP 1 Adjust intermodulation analyzer composite signal output amplitude for +4 dBm (0 vu) at machine output connector (0 dBm at audio test PWA output).
- STEP 2 Adjust intermodulation analyzer to normalize input signal, and then read intermodulation distortion. Compare readings with specifications given in Table 5-19 for tape speed and equalization standard in use.

Speed	ANSI S4.3/DIN 45507 Peak Weighted	ANSI/DIN Peak Unweighted	NAB RMS Unweighted
7.5 in/s (19.05 cm/s) 15 in/s (38.1 cm/s) 30 in/s (76.2 cm/s) Start Time: (10-1/2 in. reel)	±0.05% ±0.03% ±0.03%	±0.12% ±0.08% ±0.08%	0.06% 0.04% 0.03%
	Time to atta	in flutter spec	ification:
7.5 in/s 15 in/s	on condensor and pr	200 ms 300 ms	

Table 5-19. Flutter and Wow

STEP 3 If type of intermodulation analyzer permits, verify tape condition and validity of measurement in step <u>8</u> as follows:

500 ms

STEP 4 Remove or switch off low-frequency test signal. Intermodulation distortion reading should drop at least to 40% of reading obtained in step 3. If reading did not drop, this is indication that tape is mechanically damaged or dirty, or that some element in tape path is causing excessive amplitude fluctuation of high-frequency test signal.

#### 5-68 Flutter

30 in/s

Flutter is measured by recording and reproducing a constant frequency tone. Any nonuniform motion in the recorder/reproducer mechanism frequency modulates the tone. This modulation, called flutter, is measured with an fm demodulator within a flutter meter. The ATR-116/124 flutter specifications are measured according to standards specified by DIN 45 507 and ANSI S4.3 peak weighted and unweighted. The rms flutter is measured as specified by the NAB standard.

When performing measurements, it is possible for the record mode flutter to add or subtract from the reproduce mode flutter, depending upon the phase relationship of the recorded and reproduced signals; therefore it is necessary to play the tape several times and average the flutter meter readings.

Prior to making a flutter measurement, perform the following steps.

- STEP 1 Clean and demagnetize heads and other tape path components as described in paragraph 5-3. Flutter meters are sensitive to amplitude modulation that results from poor head-to-tape contact or from signal dropouts.
- STEP 2 Check tape tension and adjust, if necessary, as described in paragraph 5-18.
- STEP 3 The audio channel to be used for flutter measurement should be in correct alignment. If necessary, perform procedure in paragraph 5-24.
- STEP 4 Use good quality bulk-erased tape (Ampex 456 or equivalent). Use a typical reel size for tape speed in use.

The following procedure applies to the use of a Micom (Bahrs) Model 8100-W flutter meter. If a different flutter meter is used, the manufacturer's instructions should be followed.

To measure flutter, proceed as follows:

- STEP 1 If Audio Test PWA is used, connect test oscillator output of flutter meter to handle input connector and select a channel for test; connect signal input connector of flutter meter to Audio Test PWA handle output connector (Table 5-15).
- STEP 2 If Audio Test PWA is not used, connect test oscillator output of flutter meter to recorder/reproducer input connector corresponding to channel selected for test, and connect signal input connector of flutter meter to appropriate output connector (Figure 2-3).
- STEP 3 Apply power, thread a reel of bulk-erased tape on transport, and engage servos.
- STEP 4 Select input monitoring for channel being used. Adjust recorder/reproducer output level and/or flutter meter input level for required
  flutter meter input level.
- STEP 5 While in input mode (tape not moving), measure static signal flutter and verify that flutter is below level of flutter anticipated (Table 5-19). Typical levels are below 0.005% peak weighted or 0.01% unweighted.
- STEP 6 Set flutter meter to measure peak weighted and meter scale to read 0.1% full scale.

- STEP 7 Select repro monitoring mode for channel being used, place system in record mode, and record for approximately I minute. While recording, note flutter indication on flutter meter.
- STEP 8 Rewind tape to beginning of the recording, place system into play mode, and read indication on flutter meter. Repeat this step three times and average the four readings along with the reading obtained while recording (step 7). The average reading should meet the flutter specifications given in Table 5-19.

#### 5-69 CORRECTIVE MAINTENANCE

When a failure is noted, perform the appropriate head maintenance, troubleshooting, or component replacement procedure.

#### CAUTION

TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS, ALWAYS TURN RECORDER/REPRODUCER POWER OFF BEFORE REMOVING OR INSTALLING A HEAD ASSEMBLY, OR BEFORE REMOVING OR INSTALLING A PWA.

### 5-70 Head Maintenance

Head cleaning, demagnetinzing, and cleaning and lubrication of the scrape flutter idler was covered under *Preventive Maintenance*; adjustment of head azimuth was covered under *Alignment and Adjustments*. Use the following instructions to change entire head assembly or to change an individual head stack on the head assembly.

# 5-71 Changing Head Assembly

To remove head assembly, proceed as follows:

- STEP 1 Remove power from ATR-116/124.
- STEP 2 Remove head cover assembly (Figure 5-6) from transport by removing five retaining screws and carefully lifting cover straight up.
- STEP 3 Remove three head assembly retaining screws (Figure 5-33).
- STEP 4 Carefully lift head assembly straight up from the transport.

To install head assembly, proceed as follows:

- STEP 1 Carefully lower head assembly over transport to mate head PWA edges (Figure 5-34) on transport into bottom of head assembly. Lower head assembly onto transport and fully mate head connector.
- STEP 2 Fasten head assembly to transport by reinstalling the three head assembly retaining screws (Figure 5-33).

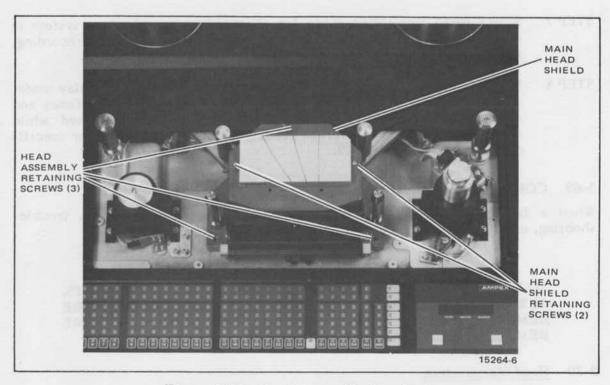


Figure 5-33. Head Assembly Installation

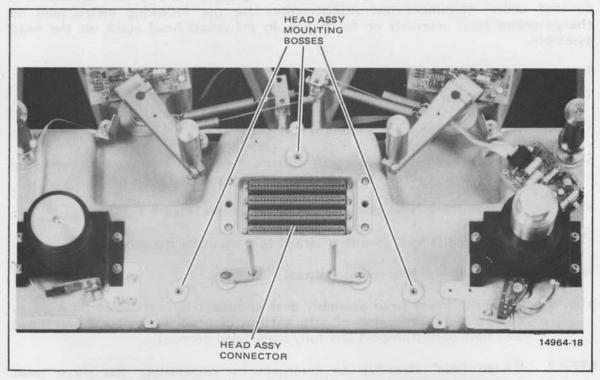


Figure 5-34. Head Assembly Connector and Mounting Bosses

### 5-72 Changing Head Stacks

To change a record, reproduce, or erase head stack, proceed as follows:

- STEP 1 Remove power from ATR-116/124.
- STEP 2 Remove entire head assembly from transport (paragraph 5-71).
- STEP 3 Remove main head shield from head assembly by removing two screws (Figure 5-33) that secure main head shield to base plate.
- STEP 4 Remove the two right-hand connector PWA retaining screws and holder (Figure 5-35).
- STEP 5 Carefully remove head stack connector(s) of the head stack to be changed.

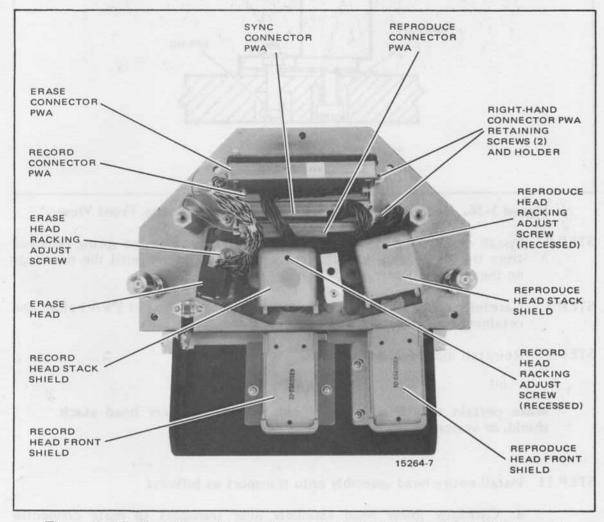


Figure 5-35. Top View of Head Assembly With Main Head Shield Removed

- STEP 6 For record or reproduce heads, remove individual head shield (Figure 5-35) from head by removing three screws from bottom of head assembly.
- STEP 7 Remove head stack mounting allen nut and spring under head stack racking adjust screw, spring, and nut behind the head stack (Figure 5-36).

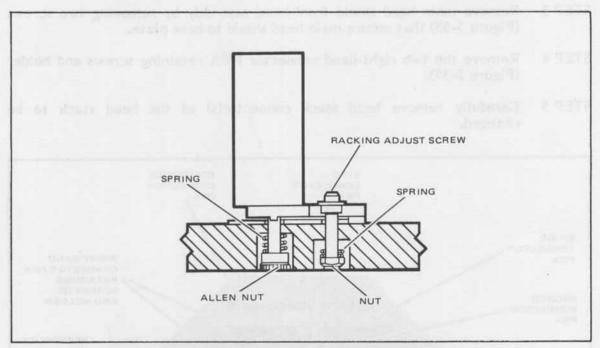


Figure 5-36. Head Assembly Spring-Loaded Pin Locations, Front View

- STEP 8 Install replacement stack with the allen nut, screws and spring removed from the above step. Install, lightly tightening screw until the nut seats on the screw shoulder.
- STEP 9 Carefully reinstall head stack connector(s) and reinstall PWA holder and retaining screws.
- STEP 10 Reinstall individual head shield.

#### Note

Make certain that head front shield fits closely over head stack shield, or system performance will be degraded.

- STEP 11 Install entire head assembly onto transport as follows:
  - a. Carefully lower head assembly over transport to mate connector PWA (Figure 5-34) to the transport.

- b. Lock head assembly to the transport by tightening the three allen head screws through holes in head assembly.
- STEP 12 Perform appropriate record, reproduce, or erase alignment procedure given in paragraph 5-24.

## 5-73 Troubleshooting

Use standard troubleshooting techniques to isolate a fault as mechanical or electrical in origin. Then proceed to isolate the fault to a certain stage or component. As an aid in locating faults, dc voltages and reference frequencies are given at many points on the schematic diagrams (Section 6), and in the theory section (Section 4) and associated block diagrams.

Performance tests can be used as an aid in diagnosing a fault. These procedures include tests for checking tape tension, absolute tape speed accuracy, speed variation, operating level, signal-to-noise ratio, harmonic distortion, intermodulation distortion, and flutter. In addition, troubleshooting hint tables and troubleshooting flow diagrams are provided in this section. Any of the corrective actions listed in the table of contents for Section 5 may be required. Recommended test equipment that may be required is listed in Table 5-1.

#### CAUTION

DO NOT REMOVE OR INSERT A PWA WITH POWER ON. TO DO SO MAY CAUSE DAMAGE TO CIRCUIT COMPONENTS. ALSO, USE EXTREME CARE NOT TO INSERT A PWA ON AN EXTENDER BOARD INTO A WRONG SLOT IN THE ELECTRONICS ASSEMBLY. THE EXTENDER BOARD IS NOT KEYED THE SAME AS THE PWA.

## 5-74 VSO Test Sequence

VSO software contains a VSO circuit test program accessed by pressing the TEST switch on the PWA. Upon completion, the test program resets the VSO. Following are the diagnostic display messages and their interpretations:

- 8085 Indicates microprocessor is barely functioning. Calls for service.
- 2716 ROM not operating properly and should be replaced. Replacement must come from Ampex.
- 8156 I/O port is not functioning properly and should be replaced.
- OSC Oscillator and/or components are not functioning properly and should be tested.

PASS VSO functioning properly. VSO not selected and is reset to 100%. This display will continue until another mode is selected.

## 5-75 VU Meter Diagnostics

Table 5-20 is a listing of possible circuit malfunctions that can be determined by the meter lamp on the VU meters. A continuous red interval during record command or a continuous amber interval outside record command indicates a normal condition. Alternate flashing of red and amber lamps of varying intervals indicates a circuit malfunction in which bias and/or erase signals should or should not be present depending on the presence or absence of the record command.

Bias	Erase	Record Command	Red Interval	Amber Interval
Present	Present	Present	Continuous	a dense appearable
Absent	Present	Present or absent	Long	Short
Absent	Absent	Present	Long	Long
Present	Absent	Present or absent	Short	Long
Present	Present	Absent	Short	Short .
Absent	Absent	Absent	_	Continuous

Table 5-20. VU Meter Diagnostics

#### 5-76 Check for Erratic Tape Timer Operation

If it is suspected that the tape timer is not operating properly in one or more of the tape speed operations, an operational check may be made with jumper J1 on the single point Search-to-Cue PWA (see Figure 2-18) set to the CD position. With jumper J1 in the CD position, the tape timer digital readout assumes the time intervals indicated in Figure 5-37.

For the least significant digit shown in Figure 5-37, the readout is a constant zero at 7.5 in/s ( $\div$  by 1); the readout rolls back to zero after a count of one at 15 in/s ( $\div$  by 2); the readout rolls back to zero after a count of three at 30 in/s ( $\div$  by 4).

For the second least significant digit shown in Figure 5-37, the readout rolls back to 10 after a count of 14 regardless of the tape speed selected. Digits 0 through 9 progress with their normal configurations displayed, but digits 10 through 14 displays the special characters indicated in Figure 5-38.

To determine whether the tape timer is functioning normally, perform the following:

- STEP 1 Place jumper J2 of the single point PWA at the CD position.
- STEP 2 Set recorder on, thread tape, and engage servos.

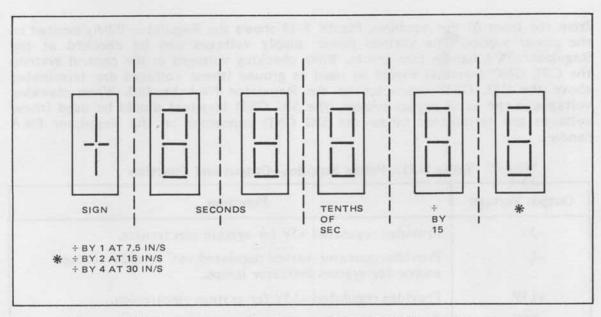


Figure 5-37. Tape Timer Readouts - J1 of STC PWA In CD Position

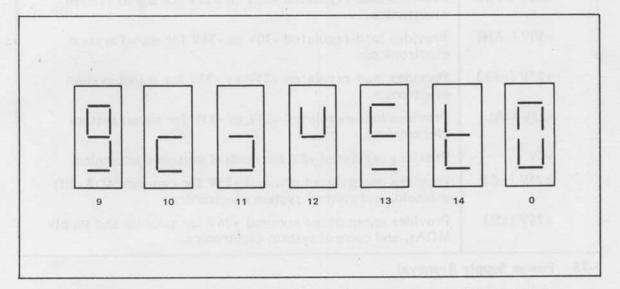


Figure 5-38. Readout Progression (Partial) for Divide-by-15 Digit Display

STEP 3 Manually rotate capstan and steadily observe tape timer increment as a reel is manually turned. Sudden jumps or other erratic behavior indicates the need for further troubleshooting.

#### 5-77 Power Supply Outputs

Table 5-21 is a list of power supply outputs and functions of these outputs. Refer to this table when checking power supply operation. These outputs may be checked

from the front of the machine. Figure 5-39 shows the Regulator PWA, located on the power supply. The various power supply voltages can be checked at the Regulator PWA handle test points. When checking voltages in the control system, the CTL GND terminal should be used as ground (these voltages are terminated above the CTL GND connector on the Regulator PWA handle). When checking voltages in the audio signal system, the SIG GND terminal should be used (these voltages are terminated below the SIG GND connector on the Regulator PWA handle).

Table 5-21. Power Supplies-Output and Function

Output Voltage	Function	
+5V	Provides regulated +5V for system electronics.	
+L	Provides operator-varied regulated +6V to +22V voltage source for system indicator lamps.	
+15V	Provides regulated +15V for system electronics.	
-15V	Provides regulated -15V for system electronics.	
+30V (+AH)	Provides load-regulated +30V to +38V for signal system electronics.	
-30V (-AH)	Provides load-regulated -30V to -38V for signal system electronics.	
+25V (+AL)	Provides load-regulated +25V to +33V for signal system electronics.	
-25V (-AL)	Provides load-regulated -25V to -33V for signal system electronics.	
+8V Provides regulated +8V for control system electron		
±25V (±C) Provides unregulated nominal ±25V for capstan N solenoid, and control system electronics.		
±26V (±R)	Provides unregulated nominal +26V for take-up and supply MDAs, and control system electronics.	

## 5-78 Power Supply Removal

#### CAUTION

DO NOT PULL PULL POWER SUPPLY OUT OF MACHINE WITHOUT FIRST DISCONNECTING POWER SUPPLY PLUGS. DAMAGE TO POWER SUPPLY CABLING MAY OTHERWISE RESULT.

To access the power supply proceed as follows:

- STEP 1 Remove electrical power from recorder.
- STEP 2 Remove lower rear panel by removing four end screws. (Do not remove screws attaching line filter to panel).

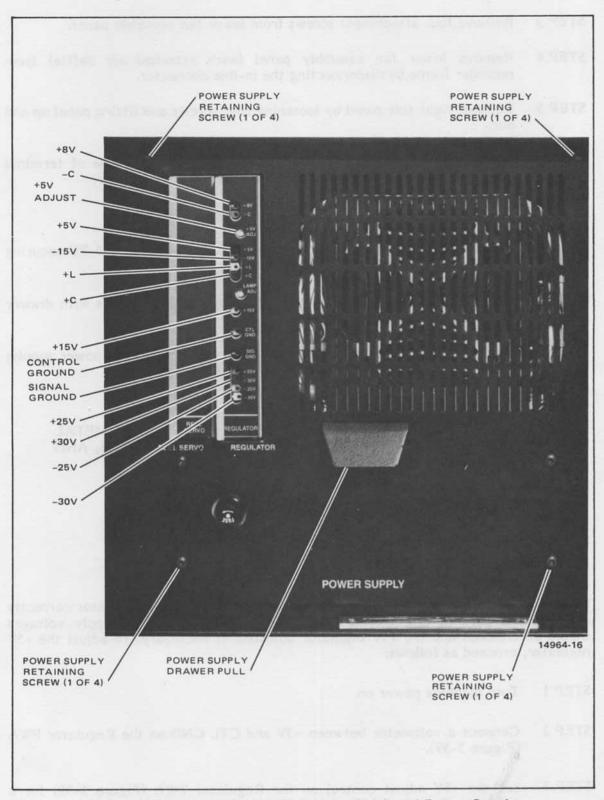


Figure 5-39. Power Supply Regulator PWA and Power Supply

- STEP 3 Remove four attachment screws from lower fan assembly panel.
- STEP 4 Remove lower fan assembly panel (with attached air baffle) from recorder frame by disconnecting the in-line connector.
- STEP 5 Remove right side panel by loosening four screws and lifting panel up and out.
- STEP 6 Remove all external connectors from power supply. Those of terminal strip TB1 are accessible after removing terminal strip cover.
- STEP 7 Disconnect ground strap at right side rear of power supply.
- STEP 8 Remove, from front of recorder, the four screws (Figure 5-39) securing power supply panel.
- STEP 9 Pull power supply fully out of recorder on supporting rails with drawer pull provided (Figure 5-39).
- STEP 10 Simultaneously press safety-catch button on each side of power supply; then remove power supply and place it near the recorder.

#### WARNING

WHEN SERVICING POWER SUPPLY AVOID CONTACT OF METAL PARTS ON TOOLS OR CLOTHING WITH TERMINALS, PINS, AND CONNECTIONS.

- STEP 11 Reconnect connections for servicing the recorder.
- STEP 12 To replace power supply, reverse removal procedures.

# 5-79 Adjustment of +5V Regulator

For proper machine operation, it is necessary to have the +5V regulator correctly adjusted. As part of any troubleshooting procedure the power supply voltages should be checked and the +5V regulator adjusted, if necessary. To adjust the +5V regulator, proceed as follows:

- STEP 1 Turn machine power on.
- STEP 2 Connect a voltmeter between +5V and CTL GND on the Regulator PWA (Figure 5-39).
- STEP 3 Set the +5V adjust control on the Regulator PWA (Figure 5-38) for a meter reading of +5.00V to +5.25V.

## 5-80 Troubleshooting Hints

Troubleshooting hints for problems associated with tape transport and tape timer are given in Tables 5-22 and 5-23, respectively. Troubleshooting hints pertaining to flutter, excessive noise or poor signal-to noise ratio, harmonic and intermodulation distortion, and general problems are given in Tables 5-24 through 5-27, respectively.

Table 5-22. Troubleshooting Hints-Tape Transport

Problem	Possible Cause/Check
Power does not switch on	Main power switch defective.
MONITORINA N. O. T. MARCHA	No main power from power source.
	Main power circuit breaker tripped.
	Thermal cutout in power relay box or power supply heat sink.
	Overvoltage on audio supply.
Power does not switch off	Main power switch defective.
Transport does not engage servos	Supply or takeup tension arm improperly adjusted.
	Defective Regulator PWA.
	Secondary fuses in power trans- former.
more assessment and the part and dollar	Reel servo malfunction.
	Reel Servo PWA not plugged into power supply card bay.
Tape slips on tape timer during	Tape tension too low.
acceleration	Tape tension unbalanced.
	Tape logic direction command wrong because of capstan tach sensor misadjustment.
	Reel servo offset misadjustment.
Tape slips on capstan forward or	Tape tension too low.
reverse direction	Tape tension greatly unbalanced.
	Tape too wide and being pinched by tension arm roller tape guides.

Table 5-22. Troubleshooting Hints—Tape Transport (Continued)

Problem	Possible Cause/Check
Tape slips on capstan forward or reverse direction (Continued)	Tape logic direction command un- stable because of capstan tach sensor misadjustment or insufficient level.
	Reel servo offset misadjustment.
Transport engages servos but no tape	Capstan motor power connection.
motion in mode	Capstan MDA malfunction.
	Capstan PWA malfunction.
Tape motion possible in fast forward and rewind modes but not play or record modes	Lockout circuitry activated because inactive recorder/reproducer speed or evaluation selected.
Tape lifter arms do not fully retract or operate in fast modes	Tape lifter arm shaft binding in pivot bushings.
	O-ring seal inside tape lifter solenoid is defective.
	Tape lifter solenoid shield not properly adjusted.
	Tape lifter solenoid driver is defective.
Tape lifter arms out too far or not far enough in fast tape modes	Individual tape lifter arm position not correct.
Tape lifter operates too slow or too fast	Solenoid air-leak control needs adjusting.
	O-ring seal in solenoid damages or binding.
Capstan does not stop rotating	Capstan tach sensor misadjusted.
	Audio PWA BCS line stuck low.
	Main CPU malfunction.
	Tape tension unbalanced.
In stop mode, capstan creeps in either direction	Tape tension unbalanced. Reel servo offset misadjustment.

Table 5-22. Troubleshooting Hints-Tape Transport (Continued)

Problem	Possible Cause/Check
Capstan does not phase lock	Tape tension incorrect.
	Tach signal is noisy.
	Reel servo offset misadjustment.
Poor tape pack in fast wind modes	Shuttle speed too high.
Tape pack height within reel incor-	Turntable height wrong.
rect (metal precision reel)	Tape tension arm guide height wrong or arm shaft is bent.
	Reel motor axis not perpendicular with tape path.
	Axis of tape guide nearest reel in question not perpendicular to tape path.
	Poorly slit or damaged tape; try another tape.
Poor takeup tape pack in play and	Very poorly slit tape.
record modes.	Axis of takeup reel motor shaft not perpendicular to tape path.
	Takeup tension arm roller not per- pendicular to tape path.

Table 5-23. Troubleshooting Hints—Tape Timer

Problem	Possible Cause/Check
Timer display accuracy incorrect in all modes	Check transport direction control logic.  Check crystal reference frequency.
	Check timer tachometer signal.
Timer accuracy incorrect only at high tape speeds	Tach sensor incorrectly adjusted.  Tape tension too low.
Timer does not reset to zero	Timer reset switch. Timer reset logic.

Table 5-24. Troubleshooting Hints-Flutter

Problem	Possible Cause/Check
Flutter out of specification	Low-frequency flutter excessive due to capstan tachometer, supply ten- sion arm tape guide, or takeup ten- sion arm tape guide.
	Poor surface quality of tape used.  Tape not bulk-erased.
	Tape tension balance incorrect.
	Capstan tachometer dirty.
	Tape guides not cleaned.
Too it a local total limited at a local total total to the page part to the page of the pa	Audio signal system alignment not correct.
	Capstan tachometer signals not set to proper phase; levels too high or too low.
	Capstan motor dragging or bearings defective.
	Capstan motor commutator dirty or damaged.
Excessive scrape flutter (high-frequency flutter)	Dirty or dry scrape flutter idler bearings. Clean and lubricate.
	Tape surface quality poor, causing uncontrollable scrape flutter.
	Scrape flutter idler position incorrect against tape.
Postalización Couscillatorion de la contraction	Scrape flutter idler not perpendicular to tape path causing tape to slide on roller.

Table 5-25. Troubleshooting Hints-Signal-to-Noise Ratio

Problem	Possible Cause/Check
Excessive system noise or signal-to- noise ratio is out of specifications	Incorrect operating level is being used.
	Incorrect noise weighting filter being used for the particular specification being measured.

Table 5-25. Troubleshooting Hints-Signal-to-Noise Ratio (Continued)

Problem	Possible Cause/Check
Excessive system noise or signal-to- noise ratio is out of specifications (Continued)	Tape that was used for recordings of a different track format not bulk erased.
	Check erase depth adjustment.
	Heads and guides not clean or demagnetized.
greater than 0.02% sout-sig etc.  Record and/or reposition operating lawels out on cornection for cycle of tape in use.	Check second harmonic distortion. If high, it could indicate magnetized component in tape path which may possibly be defective and cause high noise.
	Check that grounding straps are secure.
	Check external test equipment for ground loops.
Physically dunamed manequarity in according to a processing and the control of th	If noise is cyclic over a long period, check for noisy voltage regulator on Audio or Preamp PWAs.
	Improper ground connection within machine.
	Problem

Table 5-26. Troubleshooting Hints-Harmonic and Intermodulation Distortion

Problem	Possible Cause/Check
High second harmonic distortion	Heads and/or tape guides magnetized.
	Audio oscillator used for measurement has a second hrmonic component greater than 0.03% rms (-70 dB) for fundamental frequencies from 500 Hz to 1.0 kHz.
	System output connected to highly nonlinear load, such as overdriven level meters.
	Record amplifier malfunctioning.

Table 5-26. Troubleshooting Hints—Harmonic and Intermodulation Distortion (Continued)

Problem	Possible Cause/Check
High second harmonic distortion (Continued)	Record head in presence of large do field.
	Erase circuitry malfunctioning.
High third harmonic distortion	Audio oscillator used for measure- ment has a third harmonic component greater than 0.05% rms (-66 dB).
	Record and/or reproduce operating levels not set correctly for type of tape in use.
	Bias not set correctly. See biasing table.
High intermodulation distortion	Same causes as for high second or third harmonic distortion.
E noise is cyclic area a long period, chuck for noise entage engulator on Authorn Presson (Web.com	Physically damaged tape causing excessive amplitude fluctuation of high frequency carrier.

Table 5-27. Troubleshooting Hints-General

Problem	Possible Cause/Check
Transport control buttons on control unit do not illuminate	5 Vdc supply inoperative. Check fuse. Main CPU connector disconnected.

# 5-81 Component Replacement Procedures

# 5-82 Removing Side and Rear Panels

To replace some of the components it may be necessary to remove side or rear panels of the ATR-116/124. Use the following procedures to remove and replace these panels.

#### WARNING

DISCONNECT LINE VOLTAGE BY UNPLUGGING THE POWER CORD BEFORE REMOVING SIDE OR REAR PANELS. EXPOSED LINE VOLTAGE IS PRESENT WHEN THE PANELS ARE REMOVED.

## 5-83 Removing Side Trim Panels

To remove side panels, proceed as follows:

- STEP 1 Disconnect electrical power from recorder.
- STEP 2 Loosen but do not remove four retaining screws indicated in Figure 5-40.
- STEP 3 Lift panel up and away from machine.
- STEP 4 To replace panels, reverse removal procedure.

### 5-84 Removal of Rear Panels

To remove rear panels, proceed as follows:

- STEP 1 Disconnect electrical power from recorder.
- STEP 2 Remove four screws (Figure 5-41) from bottom rear panel.
- STEP 3 Lift panel with attached filter away from machine and set down on floor.
- STEP 4 Disconnect in-line connector from panel.
- STEP 5 Remove four screws (Figure 5-41) from lower fan panel.
- STEP 6 Lift lower fan panel with attached air deflector away from machine using care not to damage wiring harnesses.
- STEP 7 To replace panels, reverse removal procedure.

# 5-85 Replacing VU Meter Lamps

To replace VU meter lamps, refer to Figure 5-42 and proceed as follows:

- STEP 1 Remove electrical power from machine.
- STEP 2 Pull down VU meter panel by grasping panel on both sides at the finger slots and pulling.
- STEP 3 Remove VU meter shield panel by lifting it from its snap retainer.
- STEP 4 The VU meter lamps are now accessible. To remove lamps, slide lamp retainer to the side and remove lamp. Note: The sticky side of a piece of masking tape or other adhesive tape can be used to aid in removing lamp from its socket once retainer is moved.
- STEP 5 To replace lamps, reverse removal procedure.

# 5-86 Replacing VU Meters

To replace VU meters, proceed as follows:

STEP 1 Pull down VU meter panel by grasping panel on both sides at the finger slots and pulling.

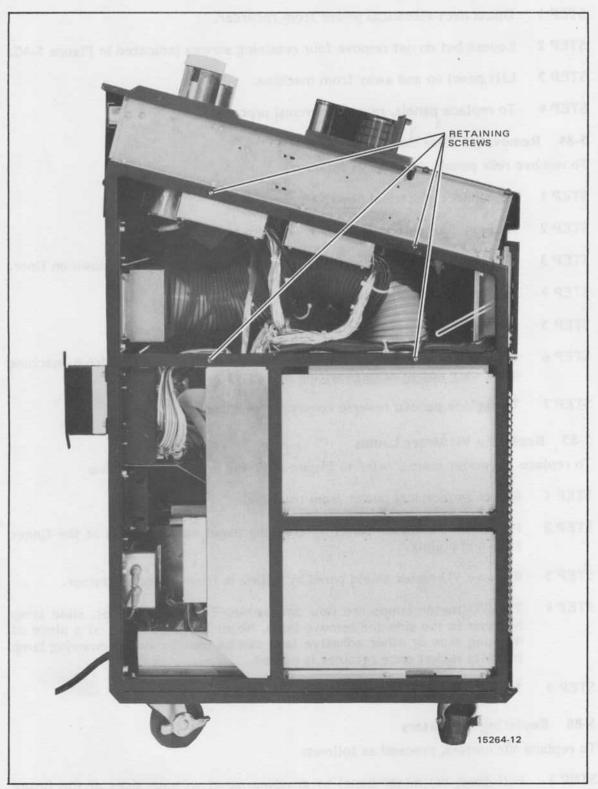


Figure 5-40. Side Panel, Retaining Screw Locations.

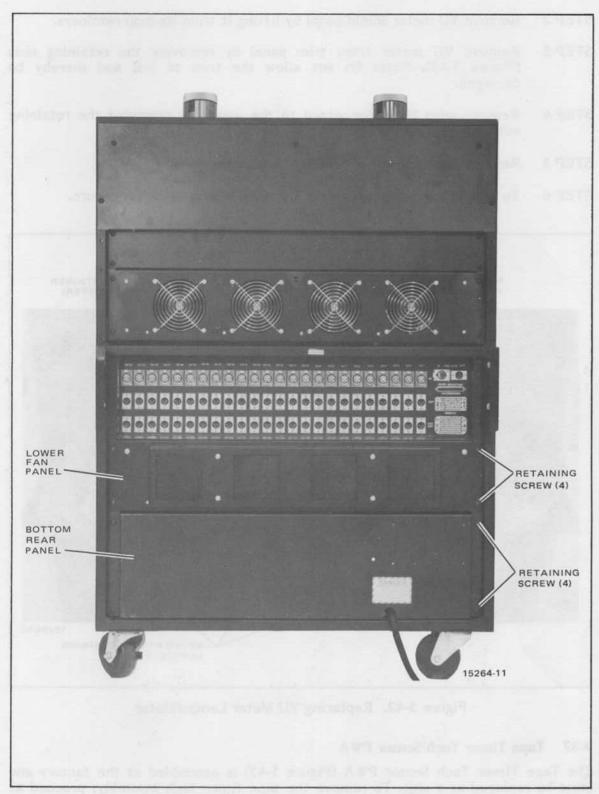


Figure 5-41. Removing Rear Panels

- STEP 2 Remove VU meter shield panel by lifting it from its snap retainers.
- STEP 3 Remove VU meter front trim panel by removing the retaining nuts (Figure 5-42). Note: Do not allow the trim to fall and thereby be damaged.
- STEP 4 Remove wire leads connected to the meter by removing the retaining nuts and connectors.
- STEP 5 Remove the meter by removing the retaining nuts.
- STEP 6 To reinstall the meter, reverse the order of the above procedure.

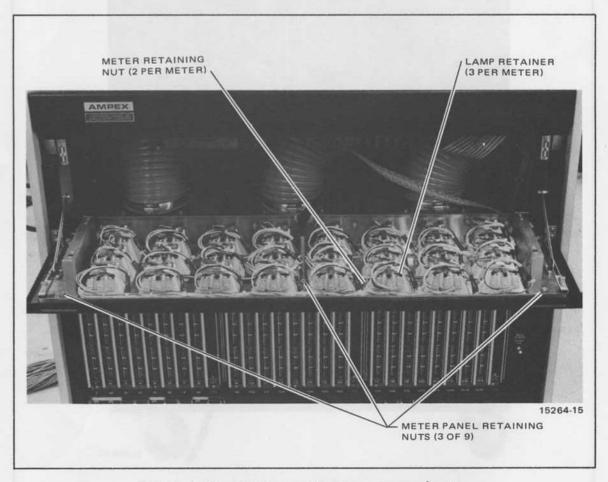


Figure 5-42. Replacing VU Meter Lamps/Meter

### 5-87 Tape Timer Tach Sensor PWA

The Tape Timer Tach Sensor PWA (Figure 5-43) is assembled at the factory and must be replaced as a unit. To remove the tape timer tach assembly, proceed as follows:

- STEP 1 Remove electrical power from machine.
- STEP 2 Remove head cover assembly (Figure 5-6) from top of transport.
- STEP 3 Remove transport overlay panel (Figure 5-6) from top of recorder/reproducer.

#### WARNING

# USE CARE WHEN HANDLING HARDWARE IN THE VICINITY OF THE TIMER DISK (FIGURE 5-44).

- STEP 4 Remove tape timer tach sensor retaining screws (Figure 5-44), and remove sensor.
- STEP 5 Disconnect tach lead connector.
- STEP 6 To reinstall, reverse order of above procedure and refer to tach alignment in this section of the manual.

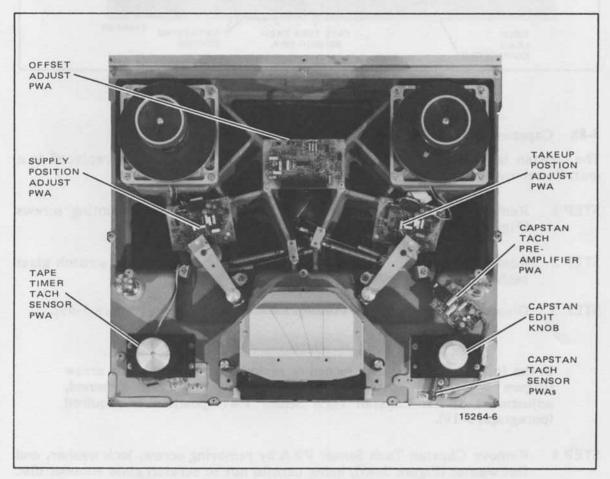


Figure 5-43. Transport Electrical Component Locations

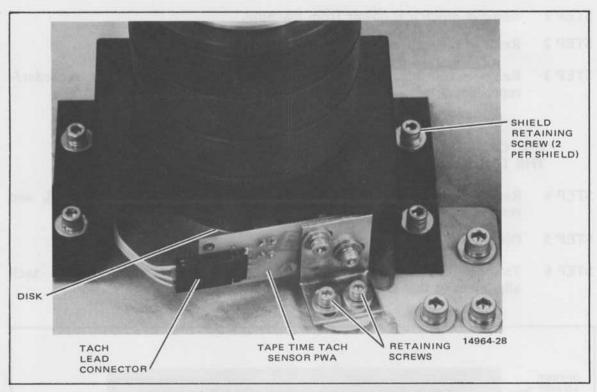


Figure 5-44. Tape Timer Tach Sensor PWA

## 5-88 Capstan Tach Assembly

The capstan tach assembly is assembled at the factory and must be replaced as a unit. To remove the capstan tach assembly, proceed as follows:

- STEP 1 Remove head cover assembly by taking out the five mounting screws (Figure 5-6).
- STEP 2 Remove the two protective shields carefully so as to not scratch glass tach disc on capstan hub.
- STEP 3 Disconnect Capstan Tach Preamp PWA lead connector (Figure 5-43).

#### Note

In the following step, do not loosen or remove the bar holddown screw (Figure 5-45) that secures the capstan sensor bar. If loosened, adjustment of the Capstan Tach Sensor PWA position is required (paragraph 5-14).

STEP 4 Remove Capstan Tach Sensor PWA by removing screw, lock washer, and flat washer (Figure 5-45), being careful not to scratch glass encoder disc or glass grating on underside of the Tape Timer Tach Sensor PWA.

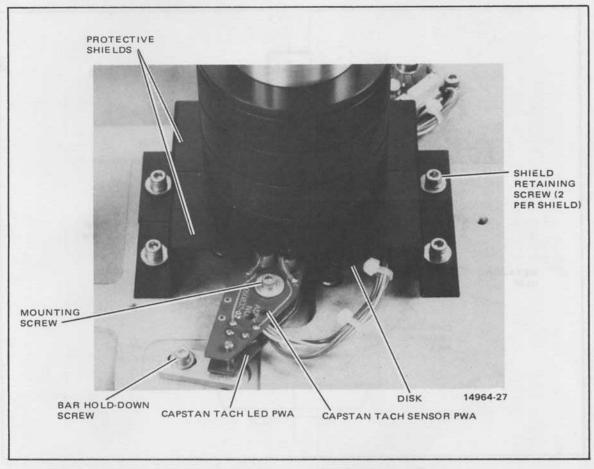


Figure 5-45. Capstan Tach Sensor PWA

- STEP 5 Remove capstan edit knob by loosening three set screws (Figures 5-43 and 5-46).
- STEP 6 Remove retaining screw and washer inside top of capstan hub.
- STEP 7 Make a pencil mark on inside of capstan hub and a corresponding one on the end of the capstan motor shaft. Make marking on the inside of the capstan hub line up with position of capstan idler set screws (Figure 5-46) (in the event a new hub is required during reassembly, the set screws of the new hub will be used for lining up the hub with the shaft). These pencil marks are used during reassembly to insure proper phasing of capstan hub on its shaft for minimum capstan hub runout and thus low flutter readings.
- STEP 8 Loosen the two capstan idler set screws on the side of the capstan hub starting with the top one first.
- STEP 9 Remove capstan hub carefully and store in a safe place. Take care to not touch glass encoder disc on capstan hub.

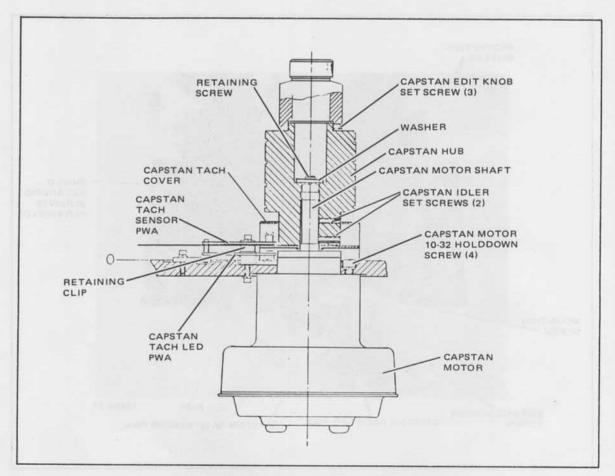


Figure 5-46. Capstan Motor Removal

#### CAUTION

IF TACH DISC NEEDS TO BE CLEANED, USE A SOFT LINT-FREE CLOTH MOISTENED WITH ISOPROPYL ALCOHOL. FOR INSTRUCTIONS REGARDING THE CLEANING OF LEDS OR ANY PHOTO-SENSITIVE DEVICE, SEE PARAGRAPH 5-3.

- STEP 10 Remove the four screws holding the Capstan Tach Preamplifier PWA to the transport casting (Figure 5-43).
- STEP 11 Replace capstan tach assembly in reverse order of removal. Line up radial alignment mark on end of motor shaft with mark on the capstan hub (or capstan idler set screws) before tightening the two set screws. This alignment position has been chosen at the factory for minimum flutter. Do not overtighten setscrews. The correct setscrew torqued is 3.0 ±0.3 lb-in. The lower set screw should be torqued first. Then, replacing screw and washer inside the hub, torque to 12 lb-in. Replace the edit knob and tighten the three set screws to 3 lb-in. Before mounting two protective shields or head cover assembly, verify that the Tach Sensor PWA is in proper position by performing the following tests:

- a. With power off, set S-2 on Capstan Servo PWA to service position.
- Apply power and press PLAY. The capstan should run at the selected speed.
- c. Press STOP and observe if capstan quickly stops.
- d. Press FAST FWD and allow capstan to reach full speed, then press STOP. The capstan should quickly stop.
- e. Press REWIND and allow capstan to reach full speed, then press STOP. The capstan should quickly stop.
- f. If the system did not pass any one of the above tests, perform the Capstan Tach Sensor PWA position adjustment procedure given in this section, paragraph 5-14.

### 5-89 Capstan Tach LED PWA

To replace the PWA LEDs, perform the following:

- STEP 1 Remove components by performing steps 1 through 9 of paragraph 5-89.
- STEP 2 Remove retaining clip and remove PWA to service the board.
- STEP 3 To reinstall, reverse removal procedures.
- STEP 4 Perform tach alignment procedure paragraph 5-14.

### 5-90 Capstan Motor and Parts Replacement

Besides the complete capstan motor, component parts that can be replaced are the motor brushes, flywheel and rotor assembly, capstan shaft assembly and capstan motor bearings (Figure 5-47). It is not necessary to remove the complete motor to replace any of these component parts. Brushes are located within the rear cover. Note that flywheel and rotor are not separable parts and therefore must be replaced as a unit.

The capstan rotor, rear cover, and brushes are manufactured by two different companies and these parts are not interchangeable on a given motor. Therefore, when parts are to be replaced be sure the correct replacement part is used.

- 5-91 <u>Capstan Motor</u>. To replace entire capstan motor, proceed as follows:
- STEP 1 Remove capstan/tach assembly as described in paragraph 5-89.
- STEP 2 Disconnect transport harness connector that connects to capstan motor connector.
- STEP 3 Remove four capstan motor mounting screws (Figure 5-46).

- STEP 4 Carefully slide motor out bottom of transport.
- STEP 5 Reinstall motor in the reverse order of removal with flat side of capstan motor housing facing the center of the transport.
- 5-92 <u>Capstan Motor Brushes.</u> Use the following procedure to replace capstan motor brushes. Motor brushes (Figure 5-48) are attached to the inside of the capstan motor rear cover. Proceed as follows:
- STEP 1 Remove only the two cover screws and flat washers shown in Figure 5-49 that secure the capstan motor rear cover to the motor (not the place screws).
- STEP 2 Note that permanent magnet within rear cover tends to hold cover to housing. Carefully pull rear cover from motor.

#### CAUTION

### DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMA-NENT MAGNET.

STEP 3 Unsolder each brush lead and remove brushes, taking care to save brush springs.

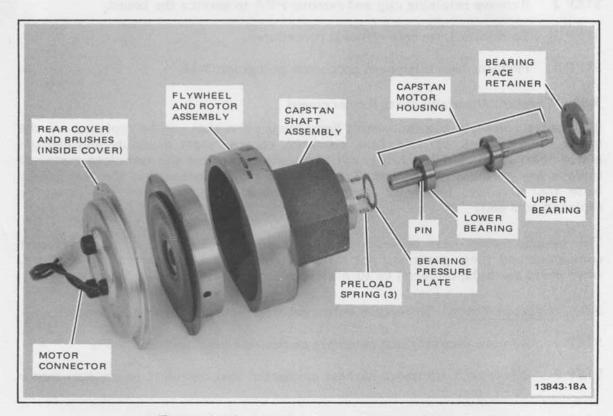


Figure 5-47. Capstan Motor Exploded View

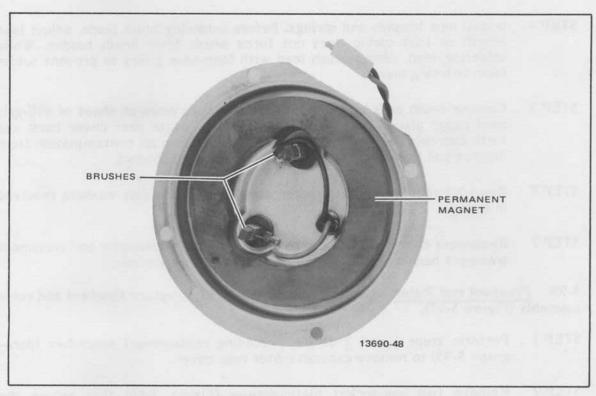


Figure 5-48. Capstan Motor Rear Cover Assembly

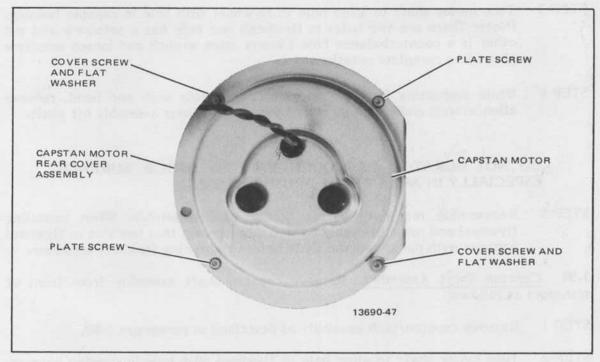


Figure 5-49. Rear View of Capstan Motor Assembly

Ampex 4890425-01



- STEP 4 Install new brushes and springs. Before soldering brush leads, adjust lead length so that spring does not force brush from brush holder. While soldering lead, clamp brush lead with long-nose pliers to prevent solder from entering braid.
- STEP 5 Contour brush ends by placing rear cover face down on sheet of 400-grit sand paper placed on a hard flat surface. Rotate rear cover back and forth approximately 90°, about five times. Clean all contamination from magnet and then clean brush ends with isopropyl alcohol.
- STEP 6 Reinstall rear cover onto motor using screws and flat washers removed in step 1.
- STEP 7 Reconnect control connector to electronics unit connector and reconnect transport harness connector to capstan motor connector.
- 5-93 Flywheel and Rotor. Use following procedure to replace flywheel and rotor assembly (Figure 5-47).
- STEP 1 Perform steps  $\underline{1}$  and  $\underline{2}$  of the preceding replacement procedure (paragraph 5-93) to remove capstan motor rear cover.
- STEP 2 Remove two hex-socket plate screws (Figure 5-49) that secure the 1/16-in. thick plate to capstan housing.
- STEP 3 Turn motor shaft to align hole in flywheel with hole in capstan housing. (Note: There are two holes in flywheel; one hole has a setscrew and the other is a counterbalance hole.) Insert allen wrench and loosen setscrew about five complete rotations.
- STEP 4 While supporting flywheel and motor assembly with one hand, remove allen wrench and carefully slide flywheel and rotor assembly off shaft.

#### CAUTION

# DO NOT SCRATCH OR TOUCH PRINTED MOTOR SURFACE, ESPECIALLY IN AREA WHERE BRUSHES SLIDE.

- STEP 5 Reassemble motor in reverse order of disassembly. When installing flywheel and rotor assembly on shaft, be certain that key slot in flywheel engages with pin in capstan shaft before tightening flywheel setscrew.
- 5-94 <u>Capstan Shaft Assembly</u>. Remove capstan shaft assembly from front of transport as follows:
- STEP 1 Remove capstan/tach assembly as described in paragraph 5-89.
- STEP 2 Turn motor shaft to align hole in flywheel with hole in capstan housing. (Note: There are two holes in flywheel; one hole has a setscrew and the



- other is a counterbalance hole.) Insert allen wrench to loosen setscrew about five complete turns. Insert a spare allen wrench in flywheel hole to maintain angular position of flywheel.
- STEP 3 Remove bearing face retainer (three screws and washers shown in Figure 5-47).
- STEP 4 From top of transport, carefully pull capstan shaft assembly up and out of capstan housing. Be careful to retain the three bearing compression springs that fit into holes in spring retainer attached to bottom of capstan housing.
- STEP 5 Prior to reinstalling capstan shaft assembly, be sure that the three bearing compression springs are in the holes in the spring retainer inside capstan housing.
- STEP 6 Check that bearing pressure plate shown in Figure 5-47 (looks like large washer) is either resting on the springs or is held by grease film to low bearing on capstan shaft assembly.

#### Note

### Do not remove grease coating within capstan housing bore.

- STEP 7 Slide capstan shaft assembly into capstan housing so that pin in side of capstan shaft assembly is aligned with setscrew in flywheel.
- Place bearing face retainer, removed in step 3, on top of upper bearing and push by hand against end of shaft to fully seat shaft in capstan housing and to compress bearing compression springs. If pin inside of capstan is not aligned with setscrew in flywheel, in order to engage key slot in flywheel, shaft will not fully insert into housing. (Approximately 20 pounds of force are required to fully compress the compression springs.)
- STEP 9 After ascertaining that shaft is correctly installed and pin is engaged in slot in flywheel, install three bearing face retainer screws and washers removed in step 3.
- STEP 10 Tighten setscrew in flywheel against capstan shaft assembly.
- STEP 11 Rotate shaft by hand to check for freedom from rubbing or binding.
- STEP 12 Reinstall capstan tach assembly as described in paragraph 5-89.
- STEP 13 Reconnect tach sensor connector to electronics assembly connector.
- 5-95 <u>Capstan Shaft Bearings</u>. With use of proper tools, new bearings may be pressed onto capatan motor shaft. If proper tools are not available and bearings need replacement, it is suggested that a new capstan motor shaft assembly

(includes bearings) be installed (Ampex Part No. 4041264). The two ball bearings used are size R8, ABEC class 5 tolerance grade (Ampex Part No. 1200075) and are pregreased and ready for use. The bearings are double shielded, but not sealed, and are greased with Andok C type grease.

To remove and replace bearings on capstan shaft, proceed as follows:

- STEP 1 Remove the capstan shaft assembly from the capstan motor housing as described in paragraph 5-95 removal procedure.
- STEP 2 Prior to removing lower bearing (Figure 5-47), remove 0.062 flywheel drive pin from the capstan shaft.
- STEP 3 Each bearing is removed by pressing bearing off shaft at end closest to bearing. Note: Removing bearings usually causes permanent damage and therefore they should not be reused.
- STEP 4 Prior to pressing new bearing on shaft, coat shaft with heavy grease to reduce friction while pressing bearing on shaft.
- STEP 5 Press new bearing on shaft by pressing squarely against bearing inner face only. If force is applied through ball bearings, the bearing will be damaged. Press bearings fully against shoulders of the shaft to obtain correct axial location relative to the shaft.
- STEP 6 If the lower bearing (Figure 5-47) was replaced, reinstall the 0.062 pin removed in step 2. Use an adhesive such as Loctite to secure pin. Be sure pin is fully bottomed in hole drilled in side of shaft.
- STEP 7 Protect capstan shaft assembly against dirt and mechanical damage until reinstalled into capstan motor housing. Reinstall capstan shaft assembly as described in paragraph 5-95 capstan shaft assembly removal procedure.

### 5-96 Reel Drive Assembly, Parts, and Adjustments

The reel drive motors are supplied by several vendors and may be used interchangeably in a supply or takeup motor position. However, brushes are not interchangeable and the correct brush for a given motor must be used.

- 5-97 Reel Drive Motor Assembly Removal and Replacement. To remove a supply or takeup reel motor assembly, proceed as follows:
- STEP 1 Remove head cover assembly by taking out five mounting screws (Figure 5-6).
- STEP 2 Remove transport top overlay panel from top of transport by removing the seven button head screws and black nylon washers (Figure 5-6).
- STEP 3 Disconnect reel tach sensor from Position Adjust PWA (Figure 5-43).

- STEP 4 Remove reel drive motor assembly from transport by removing the four mounting screws, lock washers, and flat washers.
- STEP 5 Disconnect appropriate reel drive motor connector (takeup or supply).
- STEP 6 For reel drive motor turntable repositioning see instructions in paragraph 5-99.
- STEP 7 For reel motor brush removal and replacement see instructions in paragraph 5-100.
- STEP 8 For removal and replacement of a reel drive motor see instructions in paragraph 5-101.
- STEP 9 Reassemble in reverse order of removal, being sure to have reel tach sensor toward the front of machine when mounting reel drive motor assembly on transport.
- 5-98 <u>Turntable Repositioning</u>, <u>Reel Drive Motor Assembly</u>. Whenever a reel drive motor has been removed it must be properly reinstalled and adjusted. To adjust turntable position proceed as follows:
- STEP I Remove reel drive motor assembly from transport by following instructions given in paragraph 5-98.
- STEP 2 When readjusting or removing turntable, loosen the two 1/4-28 cap screws on turntable assembly clamping collar (Figure 5-50).
- STEP 3 Adjust turntable height by first removing cover screw on top of reel holddown knob assembly, then adjusting turntable height adjustment screw to a measured height of 1.644 ± 0.0015 in. as shown in Figure 5-50.
- STEP 4 Tighten the two 1/4-28 cap screws on the turntable assembly clamping collar to a torque of 65 in-lbs and recheck the turntable height to determine if it has changed during retightening of clamping collar. If the turntable height has changed, it must be readjusted.
- STEP 5 Check turntable height on different sides for correct height and runout. If it does not meet specifications then recheck height adjustment. If that does not correct the problem then remount motor and shield assemblies through instructions in paragraph 5-101.
- STEP 6 Replace turntable cover screw using thread lock (Loctite grade C) and torque to 20 to 25 in-lbs.
- STEP 7 Reinstall the reel drive motor assembly on the transport by following instructions given in paragraph 5-98.

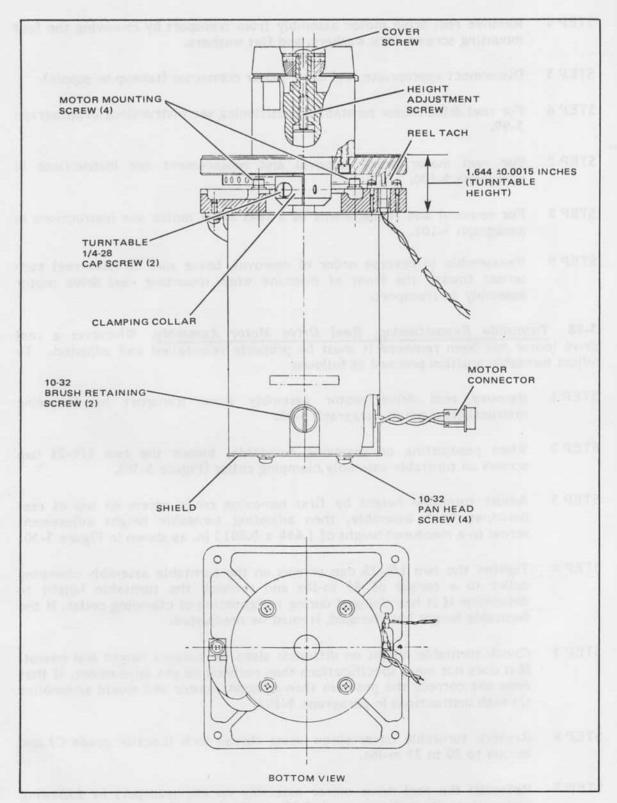


Figure 5-50. Reel Drive Motor Assembly

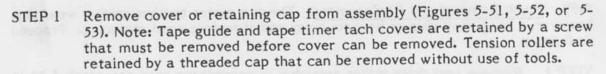
- 5-99 <u>Brush Removal and Replacement</u>. The two motor brushes seldom wear out; however, a brush may chip or become noisy and therefore need replacing. Proceed as follows:
- STEP 1 Remove reel drive motor assembly in accordance with paragraph 5-98 in this section of the manual.
- STEP 2 To remove a brush, use a large bladed screwdriver and unscrew brush retaining screw (Figure 5-50). The brush has a spring attached which maintains pressure against the motor commutator. Slide old brush out of retaining hole in motor.
- STEP 3 Clean new brush with isopropyl alcohol and install in motor.
- STEP 4 Secure new brush and spring with retaining screw removed in step 2.

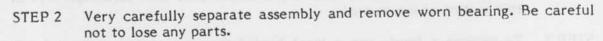
#### CAUTION

A NEW BRUSH MAY SQUEAK UNTIL MOTOR HAS BEEN RUN LONG ENOUGH TO SEAT THE NEW BRUSH TO THE COMMUTATOR. DO NOT APPLY ANY LUBRICANTS TO BRUSH.

- 5-100 Removal and Replacement of Reel Drive Motor. To remove and reinstall a reel drive motor, proceed as follows:
- STEP 1 Remove and reinstall reel drive motor assembly from transport following instructions in paragraph 5-98.
- STEP 2 Remove and reinstall knob-turntable assembly by loosening two cap screws on turntable clamping collar (Figure 5-50).
- STEP 3 Remove the bottom end motor shield by removing four pan-head screws, lock washers, and flat washers.
- STEP 4 Remove four motor retaining screws lock washers and flat washers on top of reel motor mounting plate and carefully slide reel motor out through bottom end of reel motor shield.
- STEP 5 When reinstalling replacement motor, have power connector lead facing same side of assembly as tach sensor cable and make sure slots on end of motor shield line up with motor brush service screws for ease of brush servicing.
- STEP 6 Reinstall rest of assembly in reverse order. Torque four cap screws on top of reel motor mounting plate to 29 lb-in.; then install bottom end motor shield which should be torqued to 8 lb-in.
- 5-101 Tape Guides, Tension Arm Rollers, and Tape Timer Tachometer Bearing Replacement

Should replacement of tape guide, tension roller, or tape timer tach bearings be necessary, bearings should be replaced as follows:





- STEP 3 Install new bearings; they must be properly oriented. A good procedure is to lay parts out as disassembled in the order and direction in which they occur in the assembly. Then, replace old bearing with new bearings.
- STEP 4 Reassemble the assembly and replace retaining cover or cap. Note: Refer to paragraph 5-10, for information on lubrication of bearings.

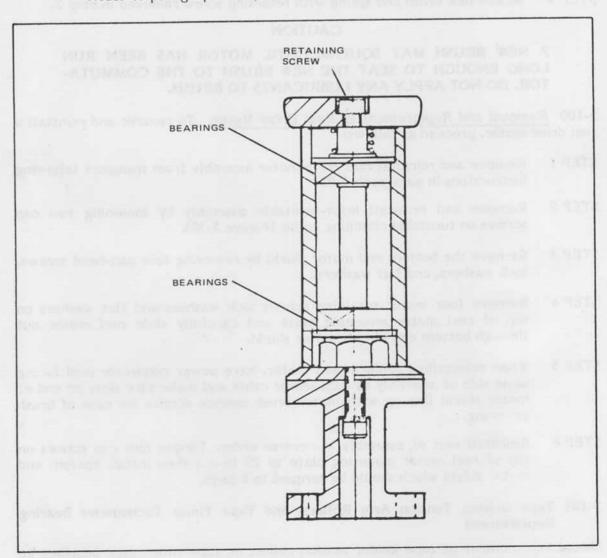


Figure 5-51. Tape Guide Bearing

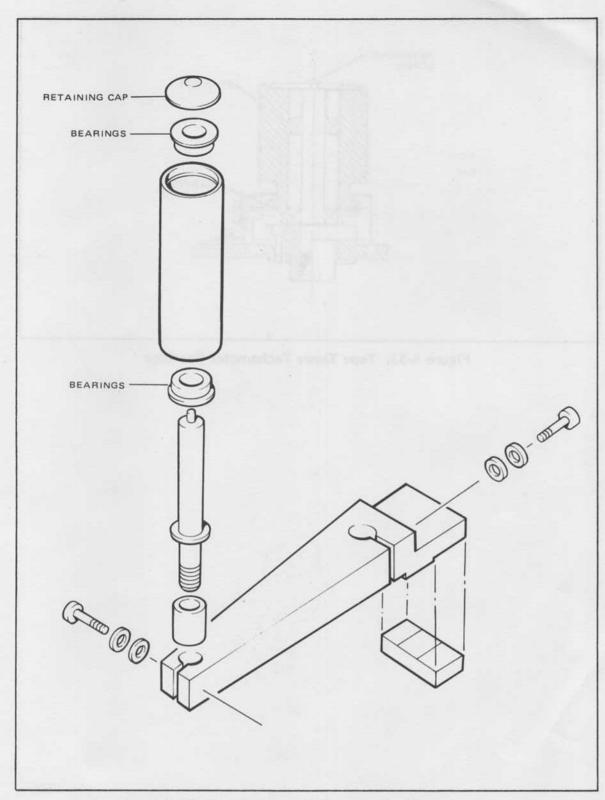


Figure 5-52. Tension Arm Roller Bearing Replacement

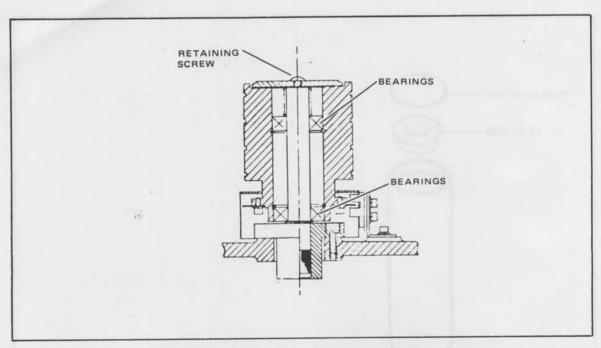


Figure 5-53. Tape Timer Tachometer Bearings

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